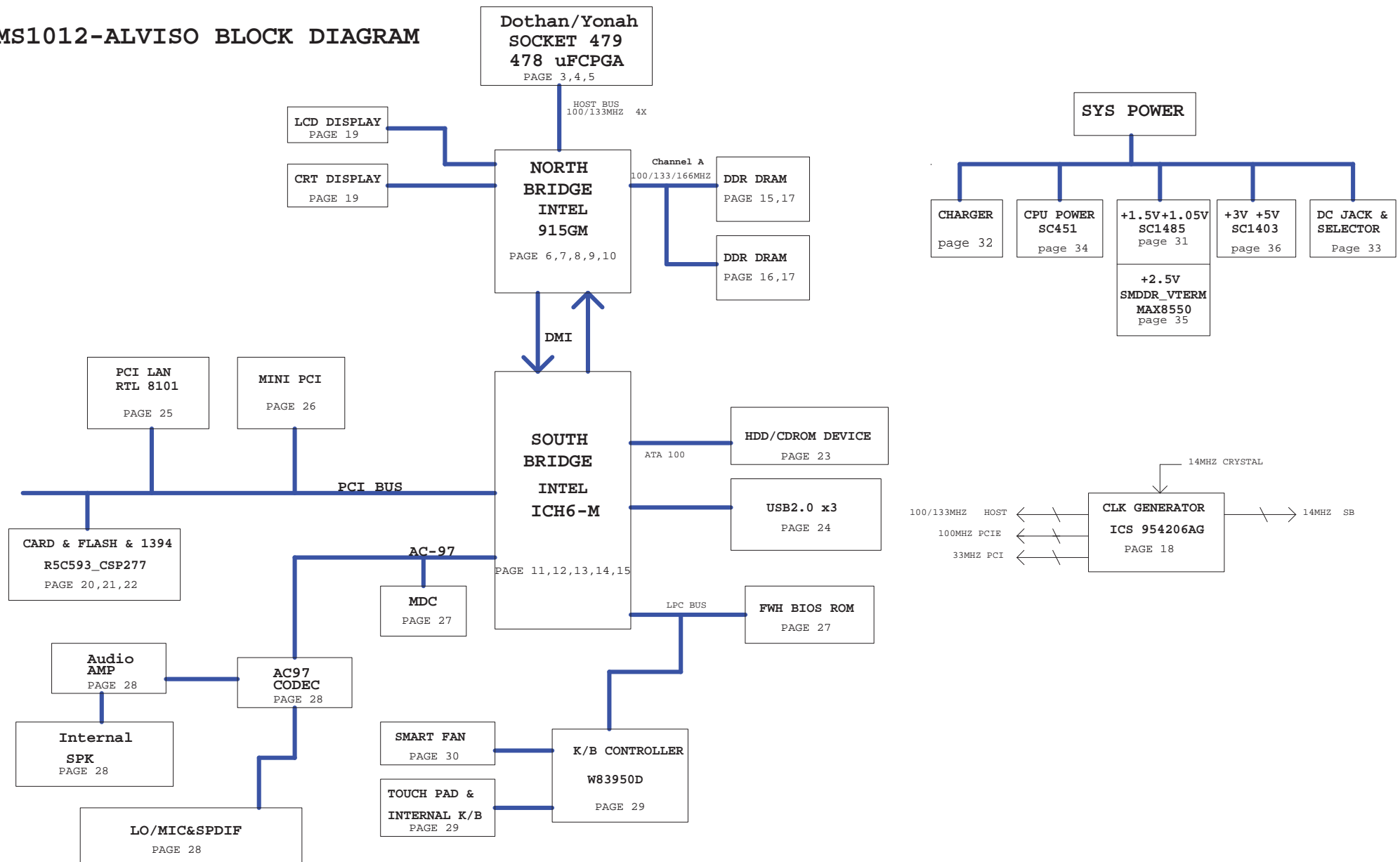


MS1012-ALVISO BLOCK DIAGRAM






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Voltage Rails

Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
VHORE	Core Voltage for Processor	GME_PWRGD
VTT	1.05 rail for Processor & Alviso I/O	RUNPWROK
SMDDR_VTERM	1.25V DDR Termination voltage (off in S4-S5)	+5VRUN
+1_5VSUS	1.5V power rail (off in S4-S5)	SUS_ON
+1_5VRUN	1.5V switched power rail(off in S3-S5)	RUN_ON
+1_8VRUN	1.8V switched power rail(off in S3-S5)	RUN_ON
+2_5VSUS	2.5V power rail DDR (off in S4-S5)	+5VSUS
+2_5VRUN	2.5V switched power rail(off in S3-S5)	RUN_ON
+3VALW	3.3V always on power rail	PWR_SRC
+3VSUS	3.3V power rail (off in S4-S5)	SUS_ON
+3VRUN	3.3V switched power rail(off in S3-S5)	RUN_ON
+5VALW	5.0V always on power rail	PWR_SRC
+5VSUS	5.0V power rail (off in S4-S5)	SUS_ON
+5VRUN	5.0V switched power rail(off in S3-S5)	RUN_ON


Voltage	Description	Control Signal
+V5_AUDIO	5.0V Power rail Audio codec(off in S3-S5)	+5VRUN

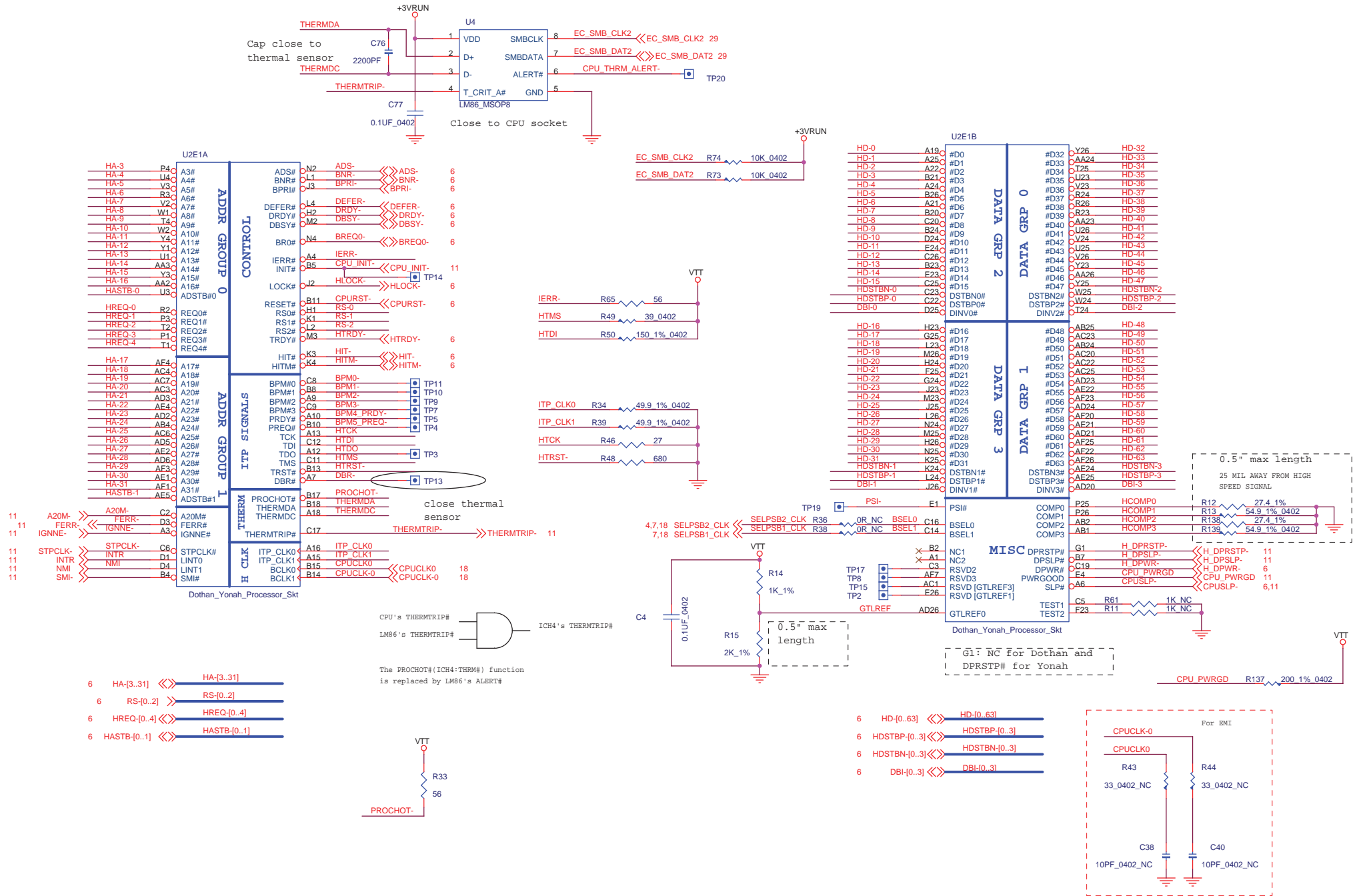
 GND	DIGTIAL GROUD	
 AGND	AUDIO GND	
 PGND	POWER Analogy GND	

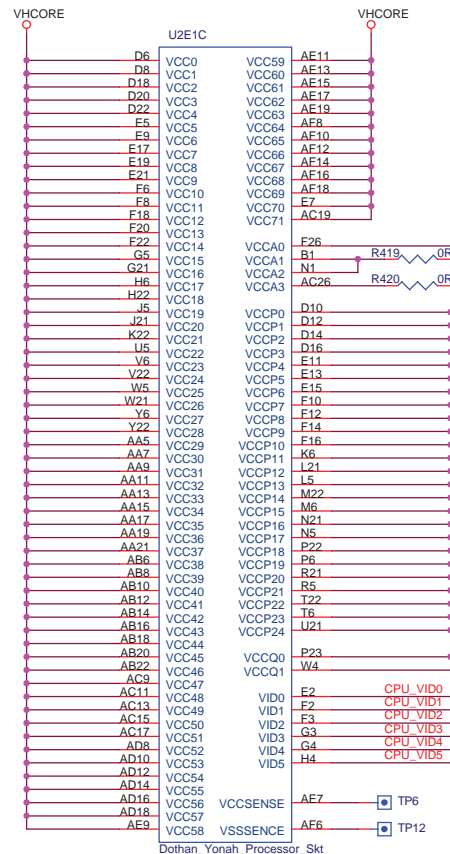
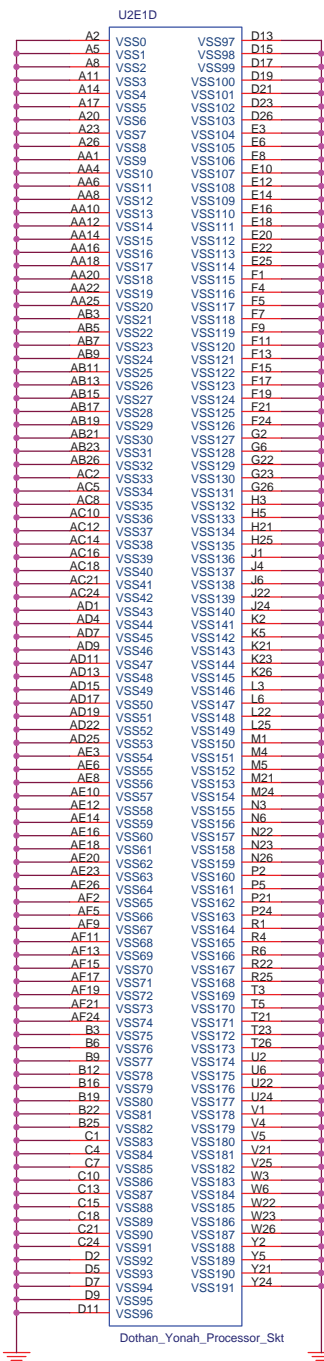
POWER STATES

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALWAYS	+V*SUS	+V*RUN	Clocks
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1M(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3(Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 / Soft OFF	LOW	LOW	LOW	ON	OFF	OFF	OFF

Note : WHEN AC MODE , System turn on then +V*SUS will always keep high

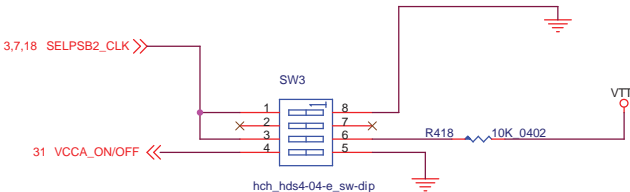
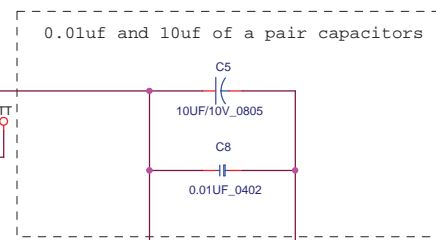
 MICRO-STAR INT'L CO.,LTD.		
Title		
PLATFORM		
Size B	Document Number	Rev 1.1
MS-1012		
Date:	Friday, January 21, 2005	Sheet 2 of 39





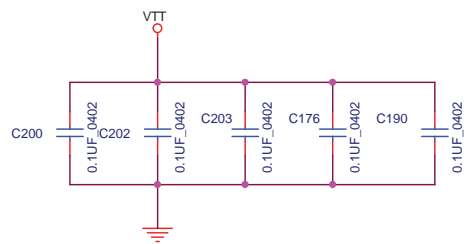
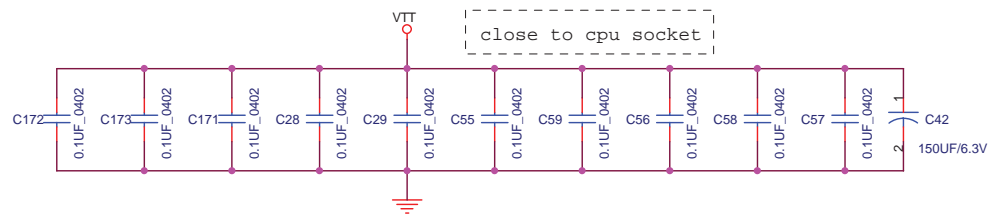
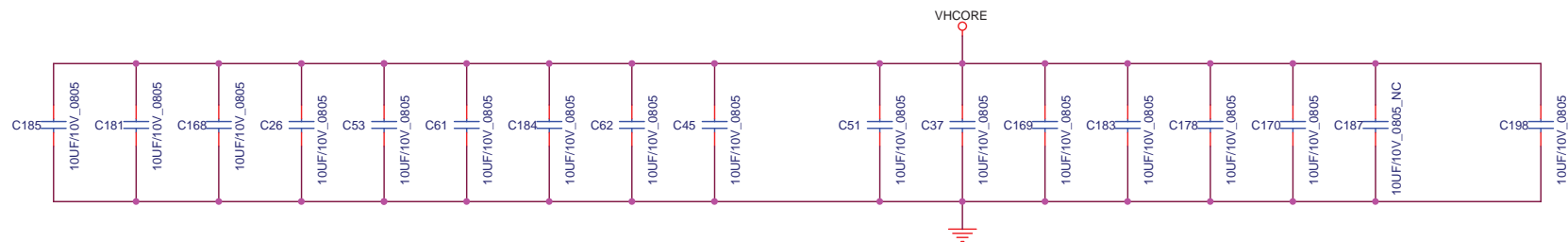
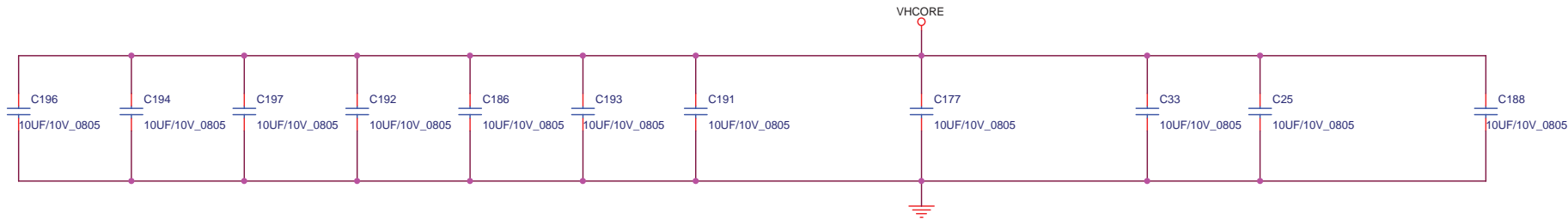
34 CPU_VID[0..5] << CPU_VID[0..5]

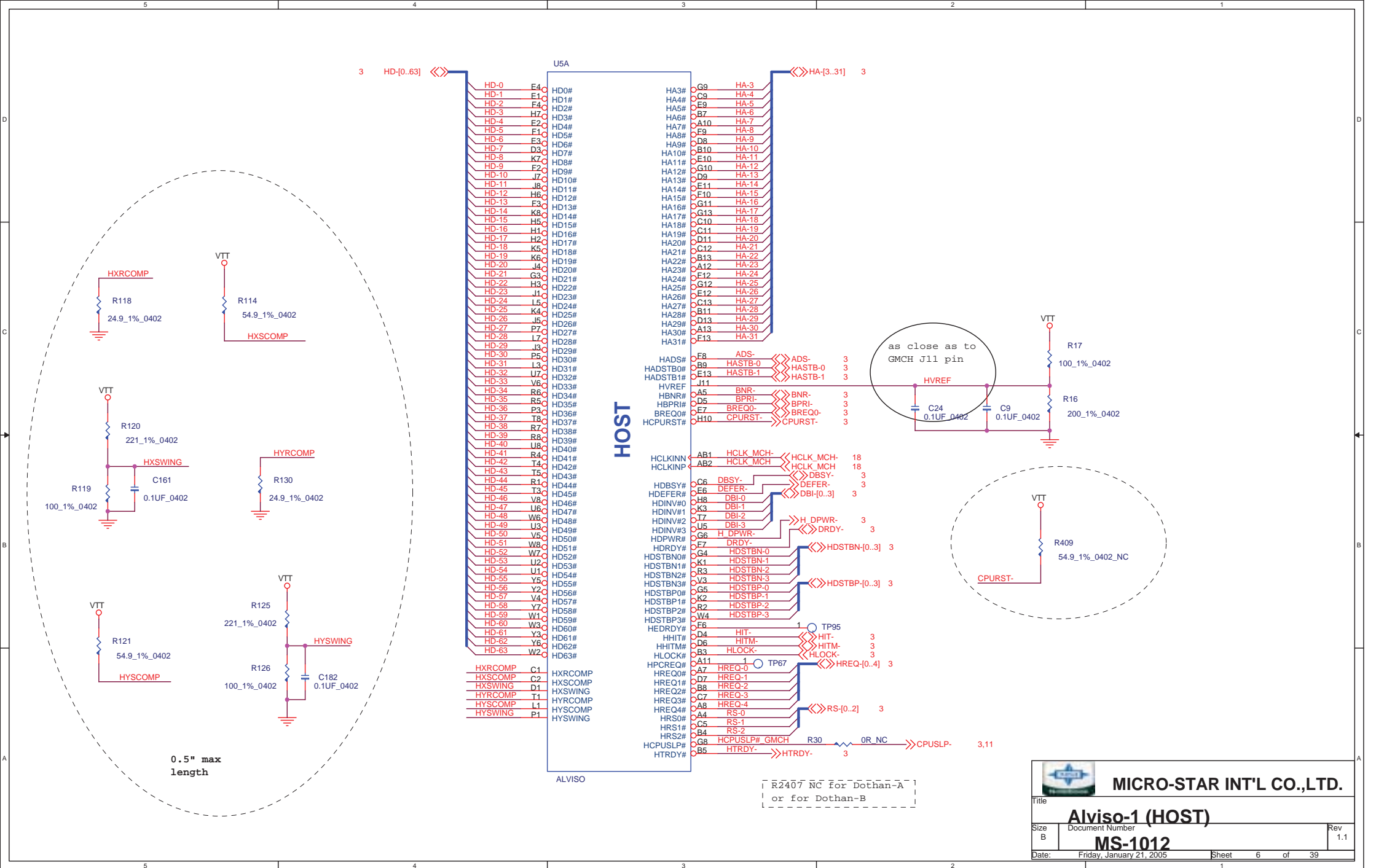
LAYOUT NOTE: Provide a test point (with no stub) to comment differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9 ohm resistors terminate the 55 ohm transmission lines.

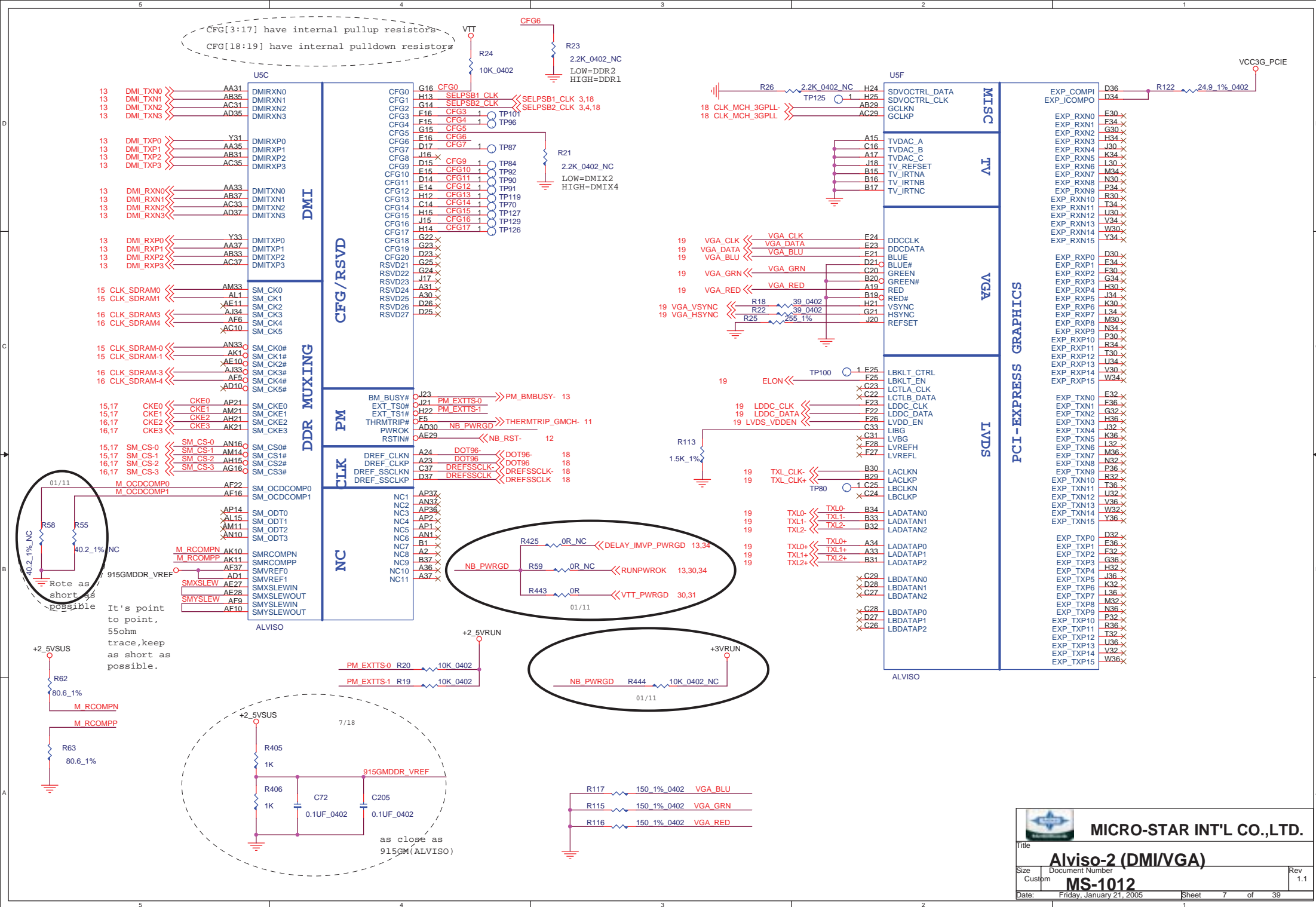


DIP4 ON CPU VCCA 1.8V

DIP4 OFF CPU VCCA 1.5V







17 R_A_MD[0..63] <<<

R_A_MD0	AG35	SADQ0
R_A_MD1	AH35	SADQ1
R_A_MD2	AL35	SADQ2
R_A_MD3	AL37	SADQ3
R_A_MD4	AH36	SADQ4
R_A_MD5	AJ35	SADQ5
R_A_MD6	AK37	SADQ6
R_A_MD7	AL34	SADQ7
R_A_MD8	AM36	SADQ8
R_A_MD9	AN35	SADQ9
R_A_MD10	AP32	SADQ10
R_A_MD11	AM31	SADQ11
R_A_MD12	AM34	SADQ12
R_A_MD13	AM35	SADQ13
R_A_MD14	AL32	SADQ14
R_A_MD15	AM32	SADQ15
R_A_MD16	AN31	SADQ16
R_A_MD17	AP31	SADQ17
R_A_MD18	AN28	SADQ18
R_A_MD19	AP28	SADQ19
R_A_MD20	AL30	SADQ20
R_A_MD21	AM30	SADQ21
R_A_MD22	AM28	SADQ22
R_A_MD23	AL28	SADQ23
R_A_MD24	AP27	SADQ24
R_A_MD25	AM27	SADQ25
R_A_MD26	AM23	SADQ26
R_A_MD27	AM22	SADQ27
R_A_MD28	AL23	SADQ28
R_A_MD29	AM24	SADQ29
R_A_MD30	AN22	SADQ30
R_A_MD31	AP22	SADQ31
R_A_MD32	AM9	SADQ32
R_A_MD33	AL9	SADQ33
R_A_MD34	AL6	SADQ34
R_A_MD35	AP7	SADQ35
R_A_MD36	AP11	SADQ36
R_A_MD37	AP10	SADQ37
R_A_MD38	AL7	SADQ38
R_A_MD39	AM7	SADQ39
R_A_MD40	AN5	SADQ40
R_A_MD41	AN6	SADQ41
R_A_MD42	AN3	SADQ42
R_A_MD43	AP3	SADQ43
R_A_MD44	AP6	SADQ44
R_A_MD45	AM6	SADQ45
R_A_MD46	AL4	SADQ46
R_A_MD47	AM3	SADQ47
R_A_MD48	AK2	SADQ48
R_A_MD49	AK3	SADQ49
R_A_MD50	AG2	SADQ50
R_A_MD51	AG1	SADQ51
R_A_MD52	AL3	SADQ52
R_A_MD53	AM2	SADQ53
R_A_MD54	AH3	SADQ54
R_A_MD55	AG3	SADQ55
R_A_MD56	AE3	SADQ56
R_A_MD57	AE3	SADQ57
R_A_MD58	AD6	SADQ58
R_A_MD59	AC4	SADQ59
R_A_MD60	AE2	SADQ60
R_A_MD61	AE1	SADQ61
R_A_MD62	AD4	SADQ62
R_A_MD63	AD5	SADQ63

U5B

DDR SYSTEM MEMORY A

ALVISO

SA_BS0#
SA_BS1#
SA_BS2#
SA_DM0
SA_DM1
SA_DM2
SA_DM3
SA_DM4
SA_DM5
SA_DM6
SA_DM7

SA_DQS0
SA_DQS1
SA_DQS2
SA_DQS3
SA_DQS4
SA_DQS5
SA_DQS6
SA_DQS7

SA_DQS0#
SA_DQS1#
SA_DQS2#
SA_DQS3#
SA_DQS4#
SA_DQS5#
SA_DQS6#
SA_DQS7#

SA_MA0
SA_MA1
SA_MA2
SA_MA3
SA_MA4
SA_MA5
SA_MA6
SA_MA7
SA_MA8
SA_MA9
SA_MA10
SA_MA11
SA_MA12
SA_MA13

SA_CAS#
SA_RAS#
SA_RCVENIN#
SA_RCVENOUT#
SA_WE#

AK15 R_A_BS0-
AK16 R_A_BS1-
AL21 1 TP192

AJ37 R_A_DM0
AP35 R_A_DM1
AL29 R_A_DM2
AP24 R_A_DM3
AP9 R_A_DM4
AP4 R_A_DM5
AJ2 R_A_DM6
AD3 R_A_DM7

AK36 R_A_DQS0
AP33 R_A_DQS1
AN29 R_A_DQS2
AP23 R_A_DQS3
AM8 R_A_DQS4
AM4 R_A_DQS5
AJ1 R_A_DQS6
AE5 R_A_DQS7

AK35
AP34
AN30
AN23
AN8
AM5
AH1
AE4

AL17 R_A_MA0
AP17 R_A_MA1
AP18 R_A_MA2
AM17 R_A_MA3
AN18 R_A_MA4
AM18 R_A_MA5
AL19 R_A_MA6
AP20 R_A_MA7
AM19 R_A_MA8
AL20 R_A_MA9
AM16 R_A_MA10
AN20 R_A_MA11
AM20 R_A_MA12
AM15 R_A_MA13

AN15 R_A_SCASA-
AP16 R_A_SRASA-
AE28 1 TP177
AE28 1 TP176
AP15 R_A_BMWEA-

R_A_BS0- 15,17
R_A_BS1- 15,17
R_A_DM[0..7] 17

R_A_DQS[0..7] 17

R_A_MA[0..13] 15,17

R_A_SCASA- 15,17
R_A_SRASA- 15,17
R_A_BMWEA- 15,17

U5G

AE31 SBDQ0
AE32 SBDQ1
AG32 SBDQ2
AG36 SBDQ3
AE34 SBDQ4
AE33 SBDQ5
AE31 SBDQ6
AE30 SBDQ7
AH33 SBDQ8
AH32 SBDQ9
AK31 SBDQ10
AG30 SBDQ11
AG34 SBDQ12
AG33 SBDQ13
AH31 SBDQ14
AJ31 SBDQ15
AK30 SBDQ16
AJ30 SBDQ17
AH29 SBDQ18
AH28 SBDQ19
AK29 SBDQ20
AH30 SBDQ21
AH27 SBDQ22
AG28 SBDQ23
AE24 SBDQ24
AG23 SBDQ25
AJ22 SBDQ26
AK22 SBDQ27
AH24 SBDQ28
AH23 SBDQ29
AG22 SBDQ30
AJ21 SBDQ31
AG10 SBDQ32
AG9 SBDQ33
AG8 SBDQ34
AH8 SBDQ35
AH11 SBDQ36
AH10 SBDQ37
AJ9 SBDQ38
AK9 SBDQ39
AJ7 SBDQ40
AK6 SBDQ41
AJ4 SBDQ42
AH5 SBDQ43
AK8 SBDQ44
AJ8 SBDQ45
AJ5 SBDQ46
AK4 SBDQ47
AG5 SBDQ48
AG4 SBDQ49
AD8 SBDQ50
AD9 SBDQ51
AH4 SBDQ52
AG6 SBDQ53
AE8 SBDQ54
AD7 SBDQ55
AC5 SBDQ56
AB8 SBDQ57
AB6 SBDQ58
AA8 SBDQ59
AC8 SBDQ60
AC7 SBDQ61
AA4 SBDQ62
AA5 SBDQ63

ALVISO

SB_BS0#
SB_BS1#
SB_BS2#

SB_DM0
SB_DM1
SB_DM2
SB_DM3
SB_DM4
SB_DM5
SB_DM6
SB_DM7

SB_DQS0
SB_DQS1
SB_DQS2
SB_DQS3
SB_DQS4
SB_DQS5
SB_DQS6
SB_DQS7

SB_DQS0#
SB_DQS1#
SB_DQS2#
SB_DQS3#
SB_DQS4#
SB_DQS5#
SB_DQS6#
SB_DQS7#

SB_MA0
SB_MA1
SB_MA2
SB_MA3
SB_MA4
SB_MA5
SB_MA6
SB_MA7
SB_MA8
SB_MA9
SB_MA10
SB_MA11
SB_MA12
SB_MA13

SB_CAS#
SB_RAS#
SB_RCVENIN#
SB_RCVENOUT#
SB_WE#

AJ15 R_B_BS0-
AG17 R_B_BS1-
AG21 1 TP184

AF32
AK34
AK27
AK24
AJ10
AK5
AE7
AB7

AF34
AK32
AJ28
AK23
AM10
AH6
AF8
AB4

AF35
AK33
AK26
AJ23
AJ10
AH7
AE7
AB5

AH17 R_B_MA0
AK17 R_B_MA1
AH18 R_B_MA2
AJ18 R_B_MA3
AK18 R_B_MA4
AJ19 R_B_MA5
AK19 R_B_MA6
AH19 R_B_MA7
AJ20 R_B_MA8
AH20 R_B_MA9
AJ16 R_B_MA10
AG18 R_B_MA11
AG20 R_B_MA12
AG15 R_B_MA13

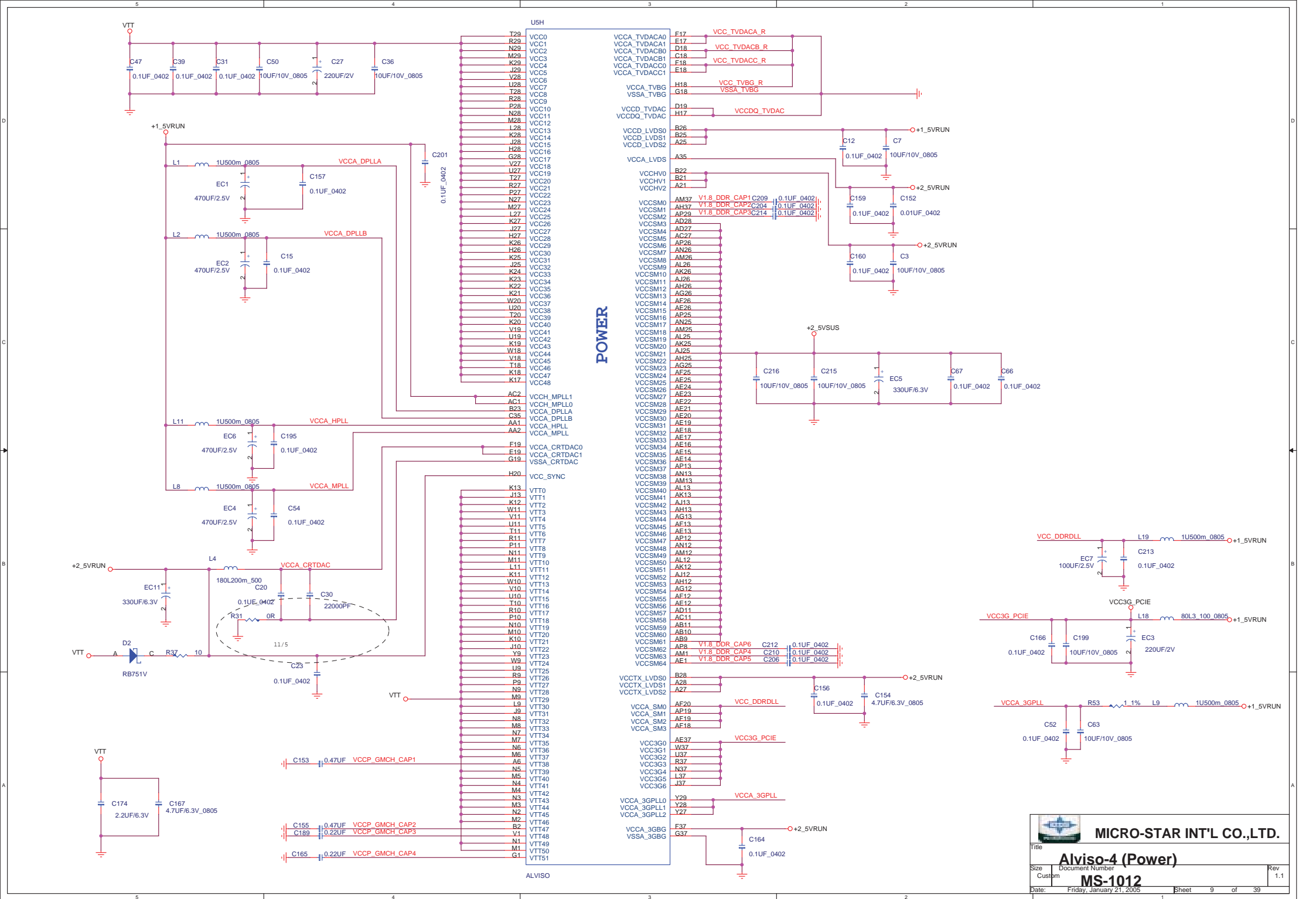
AH14 R_B_SCASA-
AK14 R_B_SRASA-
AE15 1 TP180
AE14 1 TP182
AH16 R_B_BMWEA-

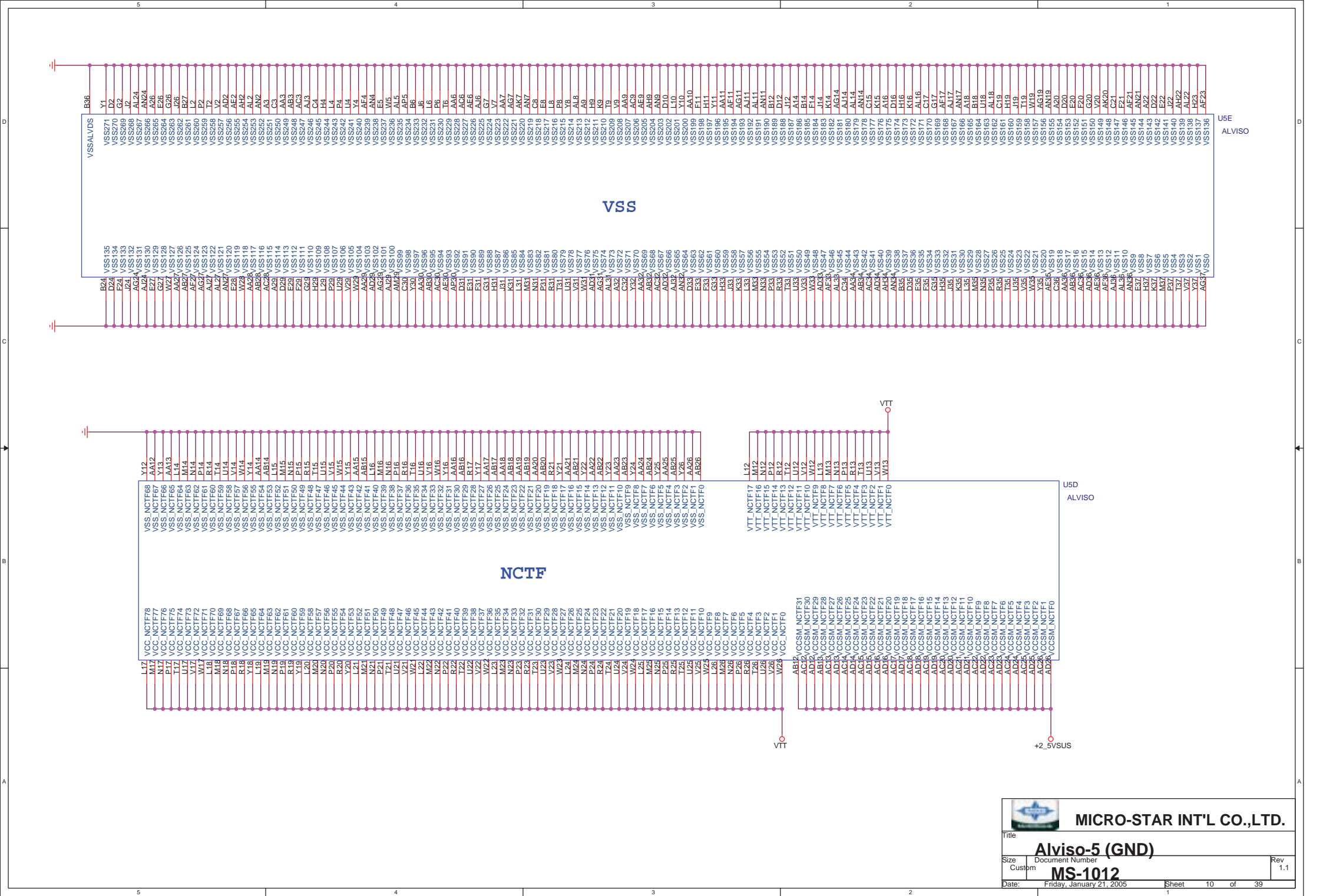
R_B_BS0- 16,17
R_B_BS1- 16,17
R_B_BS2- 16,17
R_B_DM[0..7] 16,17
R_B_DQS[0..7] 16,17
R_B_MA[0..13] 16,17
R_B_SCASA- 16,17
R_B_SRASA- 16,17
R_B_BMWEA- 16,17

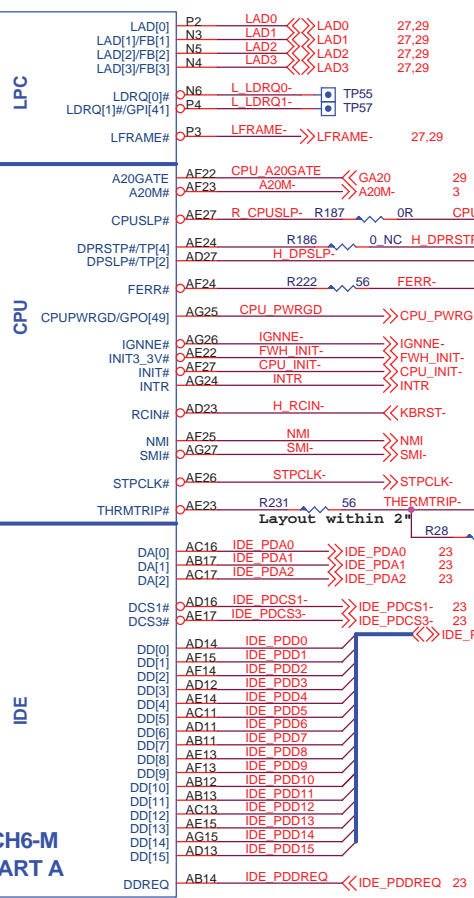
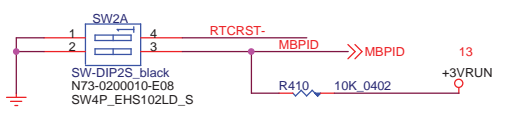
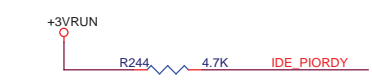
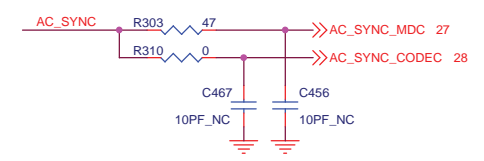
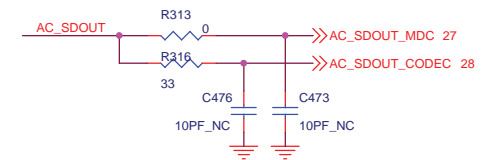
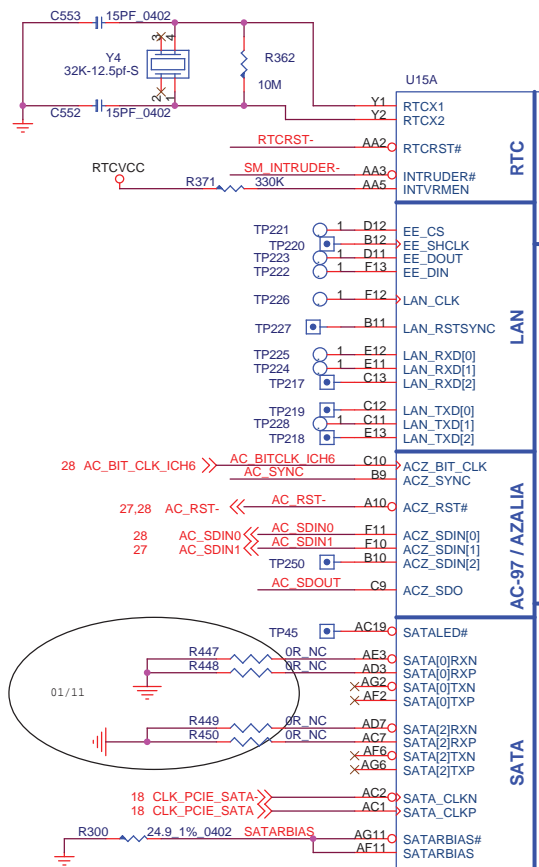
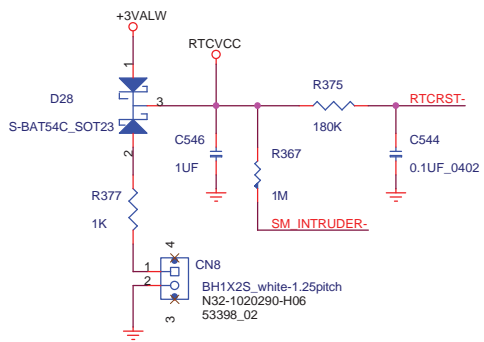


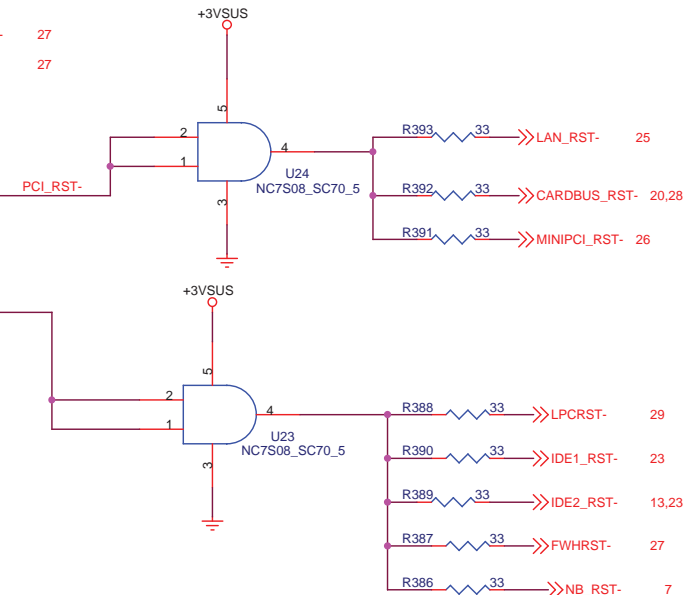
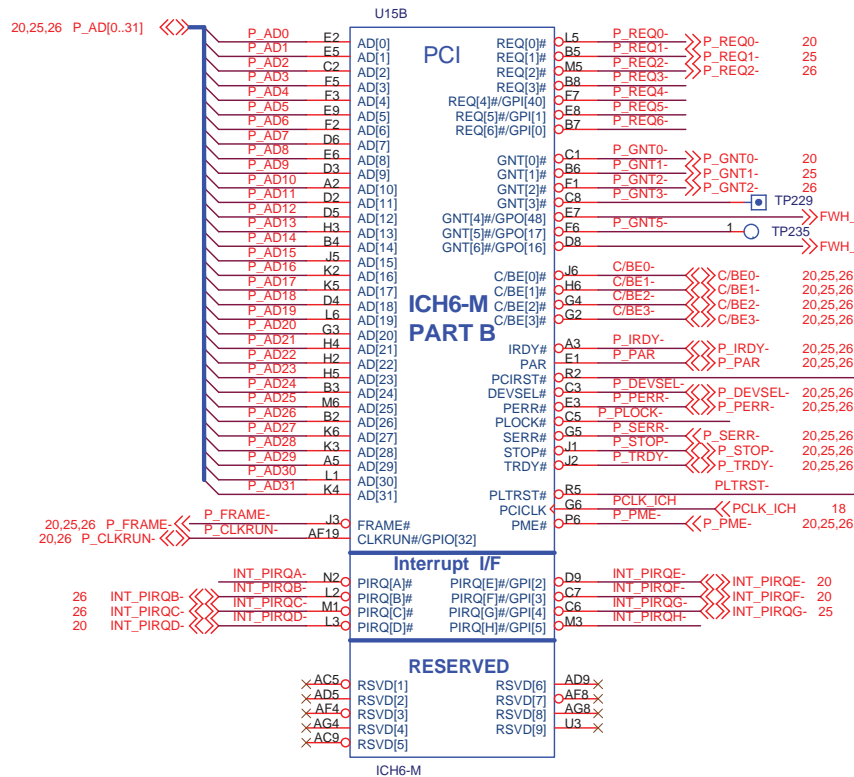
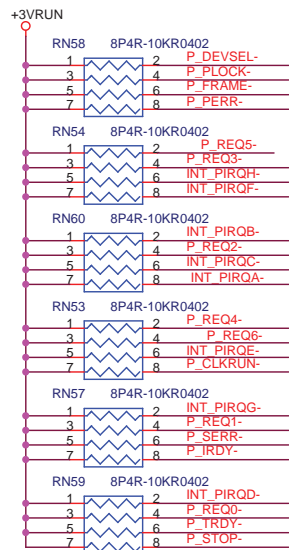
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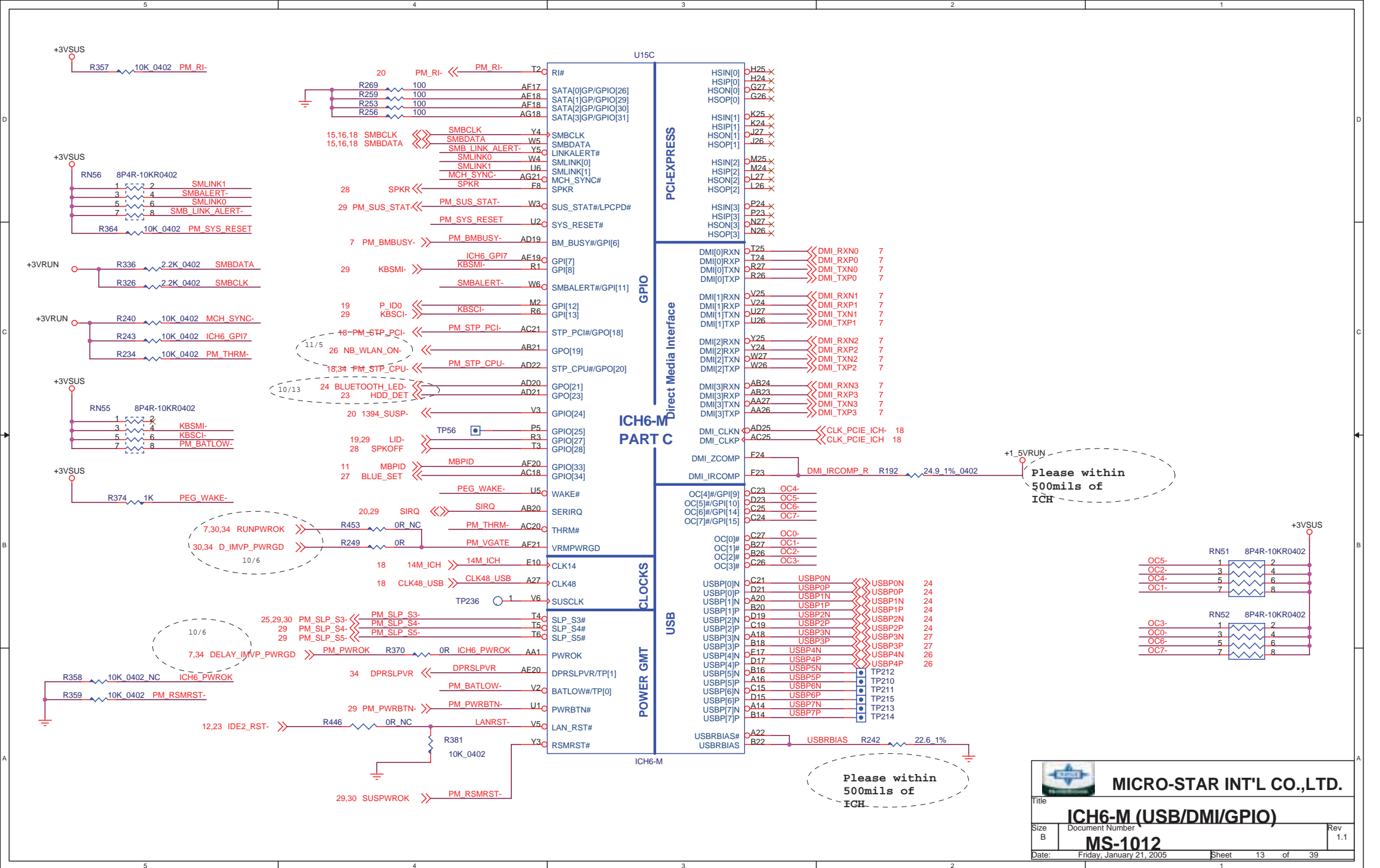
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Alviso-3 (DDR)		
Size	Document Number	Rev
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Date:	Friday, January 21, 2005	Sheet 8 of 39

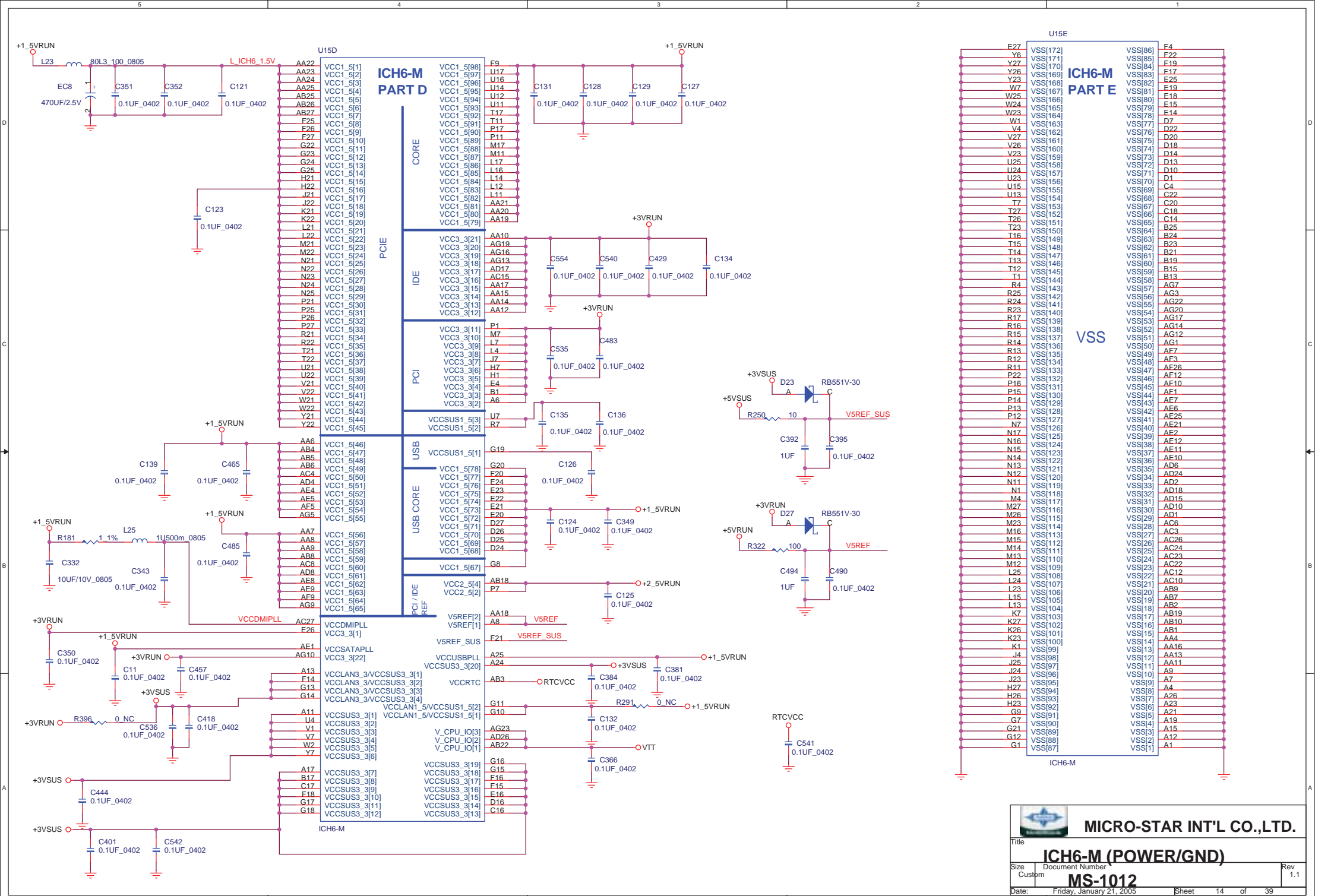


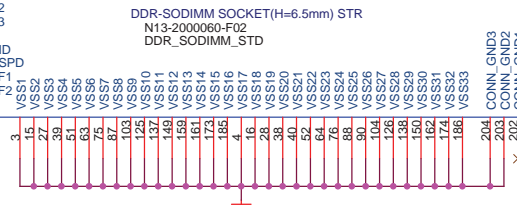
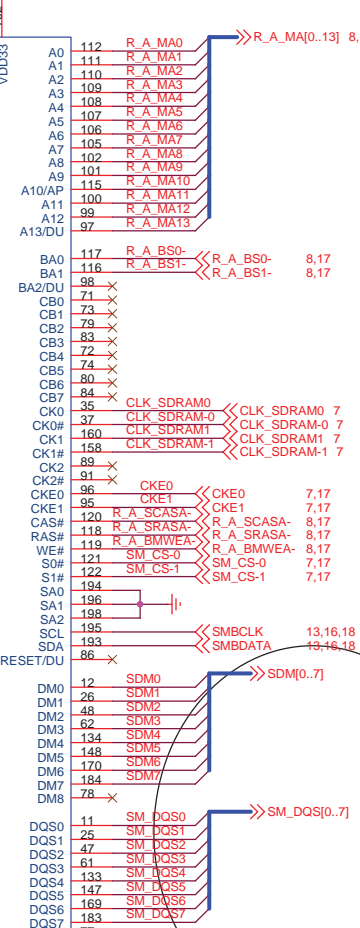
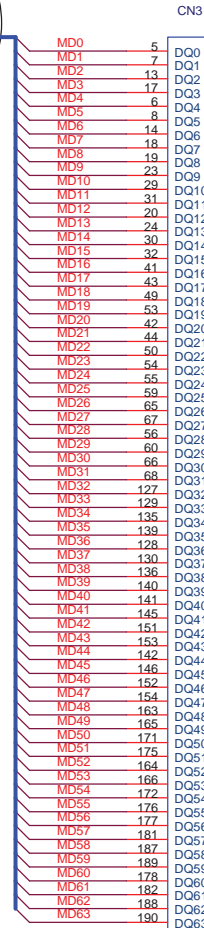
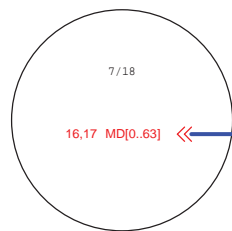




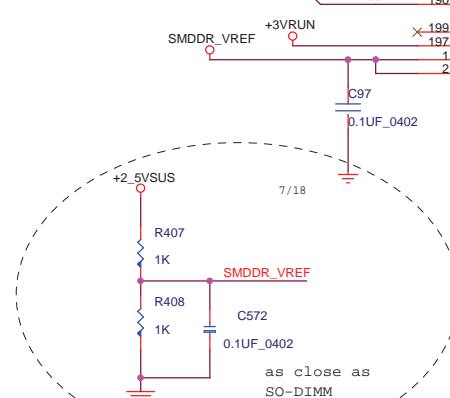
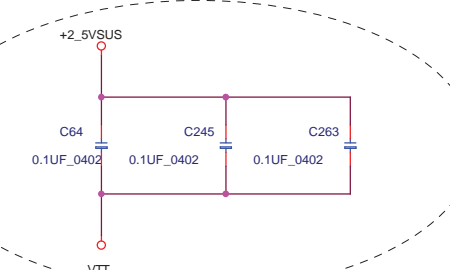
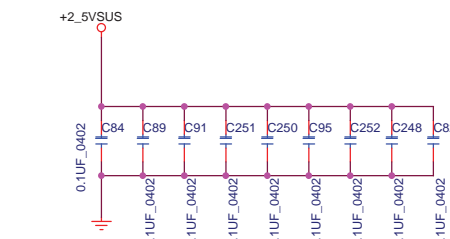
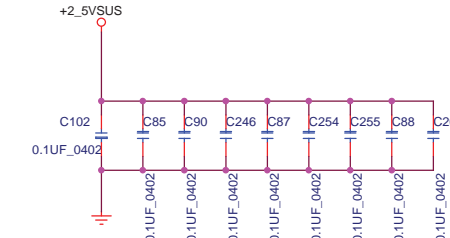
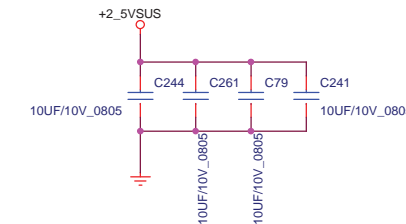


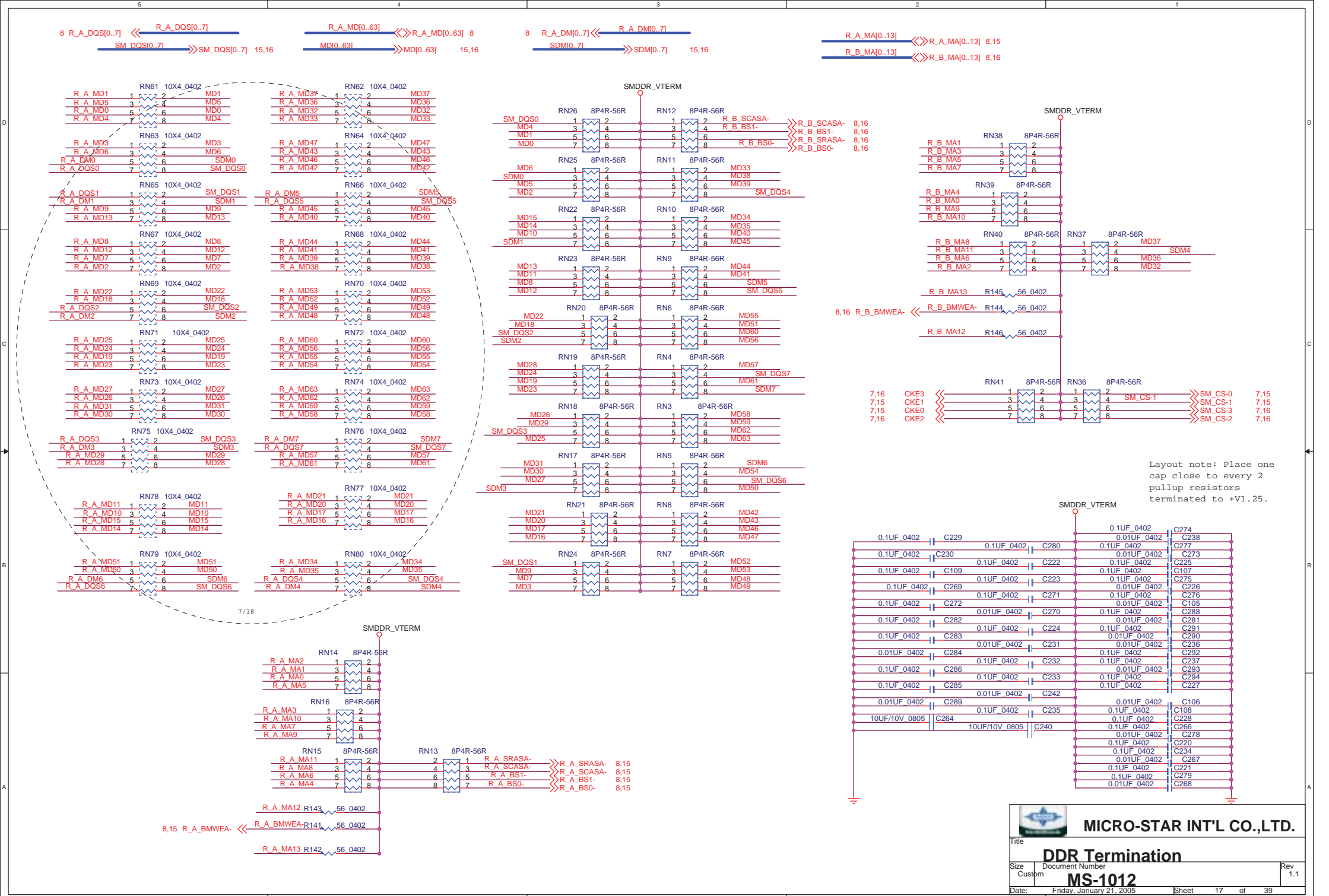


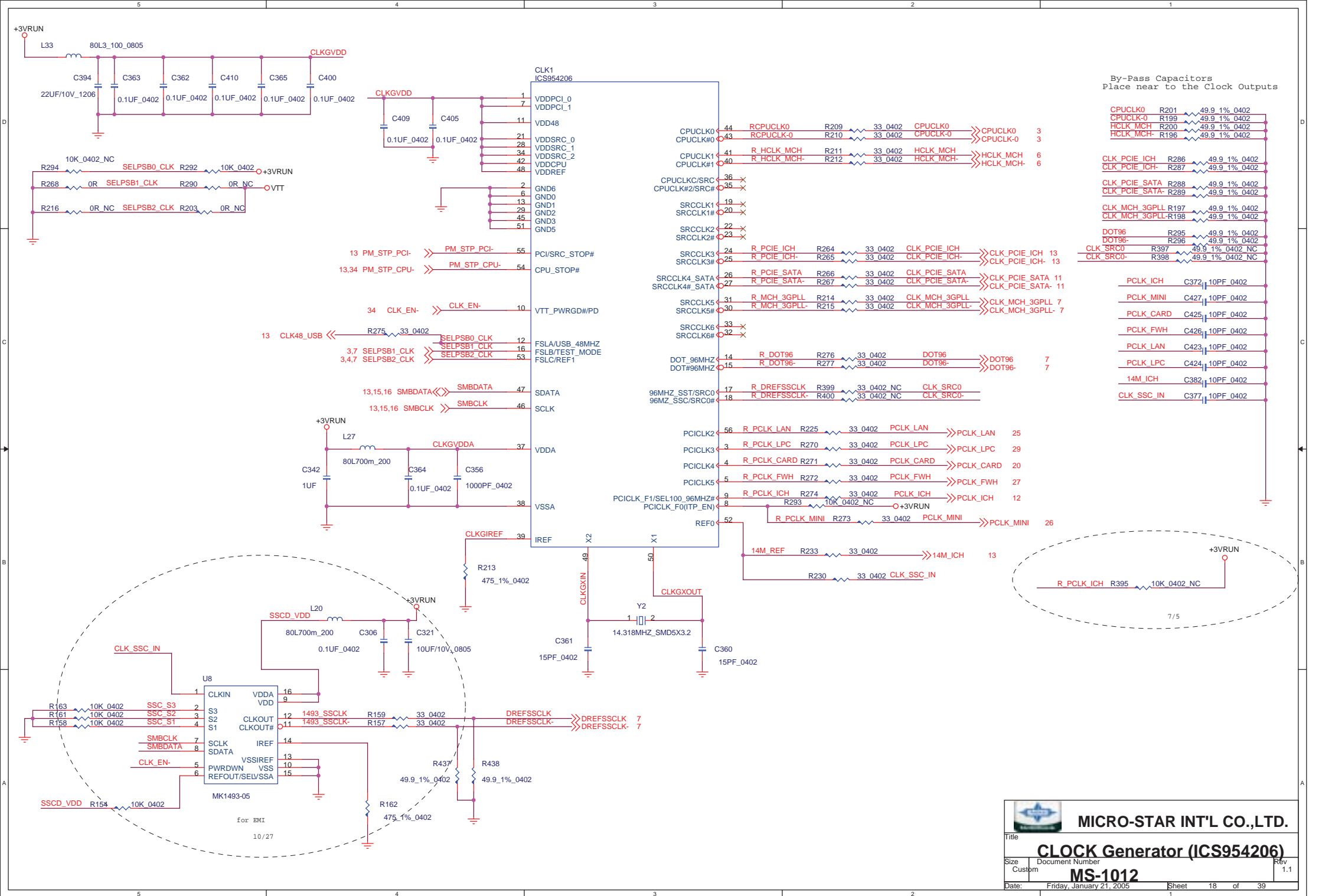


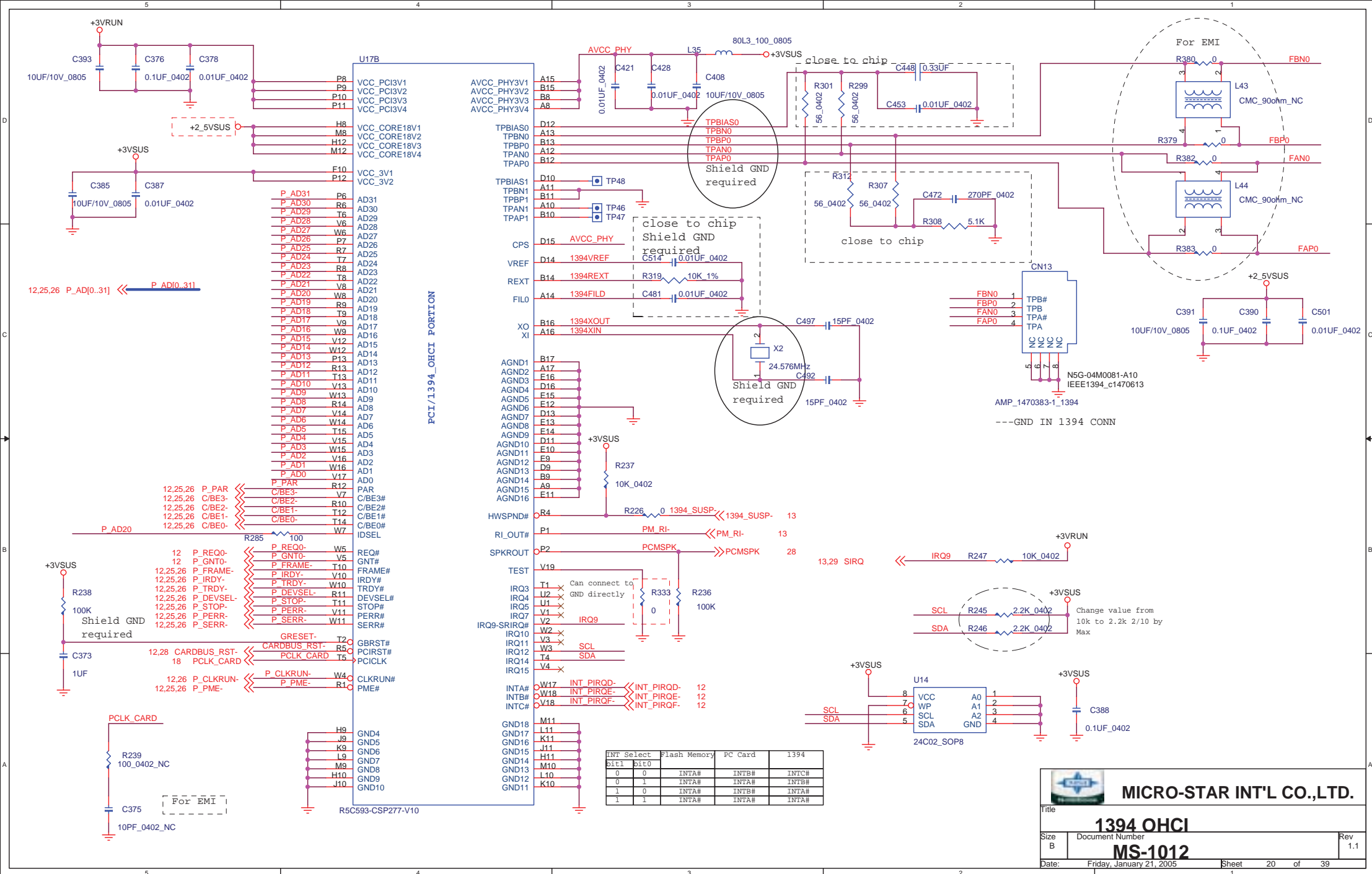


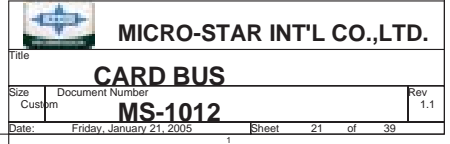
Layout note: Place capacitors between and near DDR connector if possible.

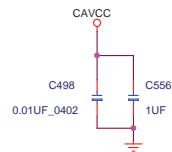




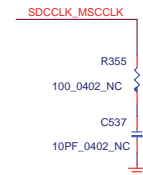
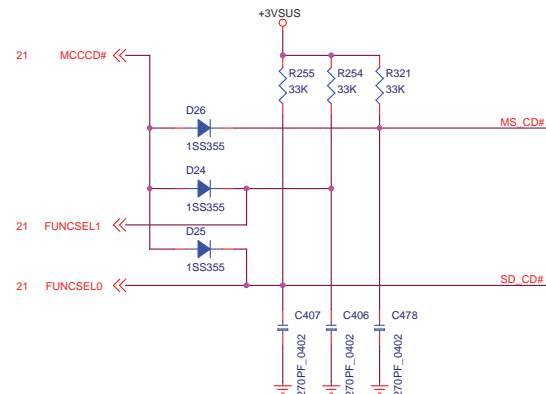


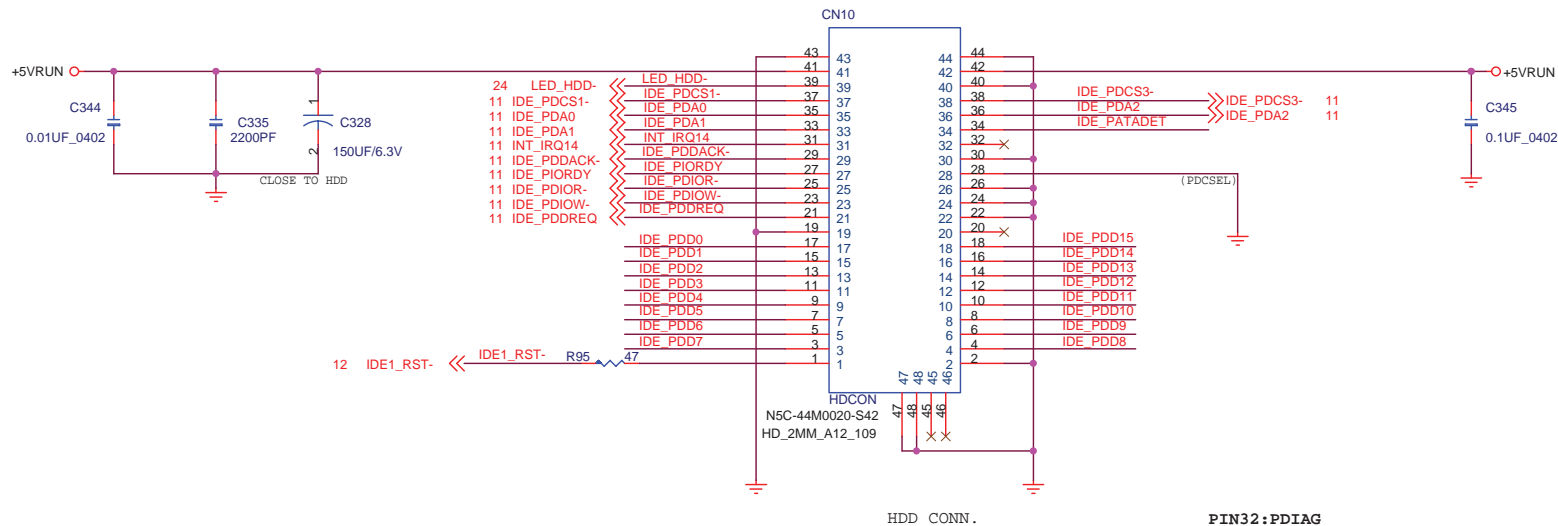




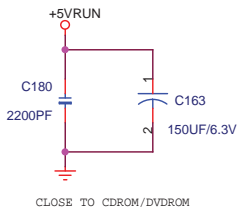
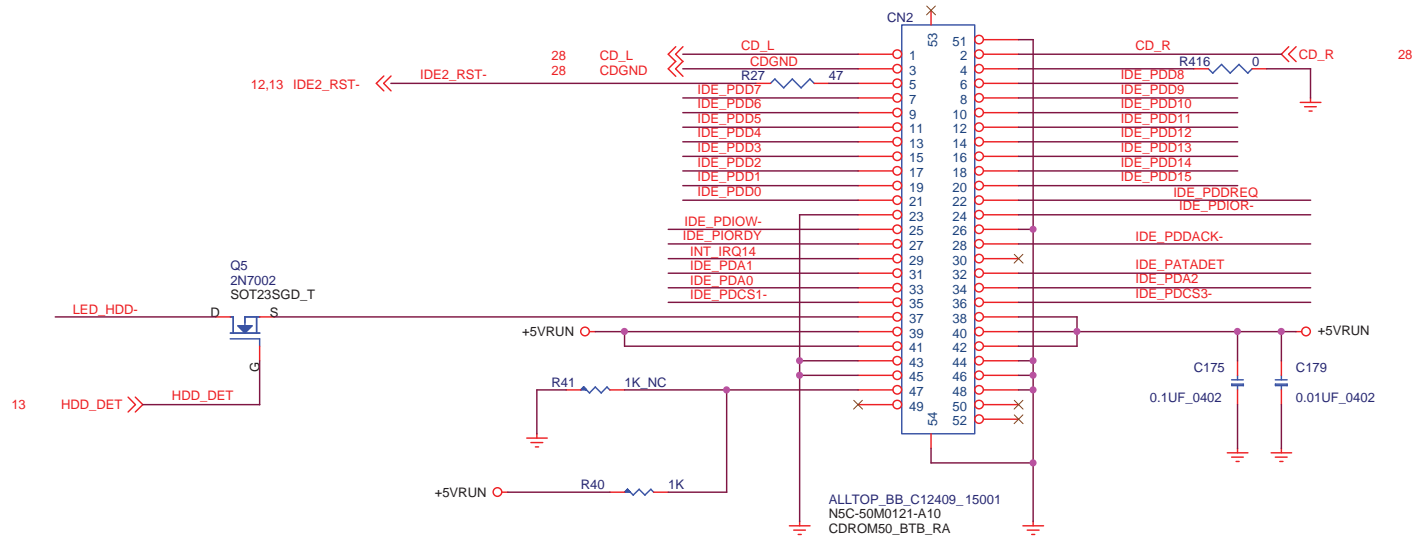
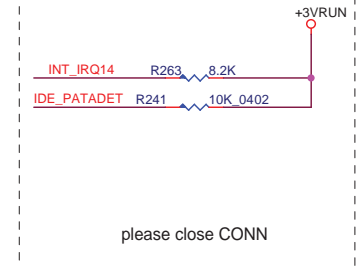



DO NOT INSERT SMARTMEDIA, SD/MMC AND MEMORYSTICK SIMULTANEOUSLY.

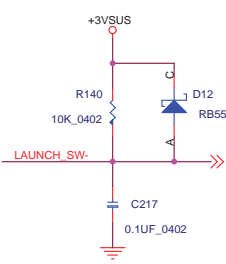
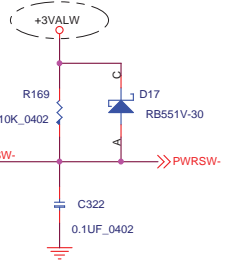
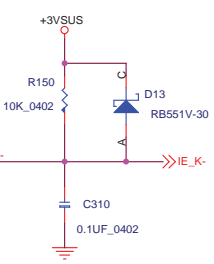
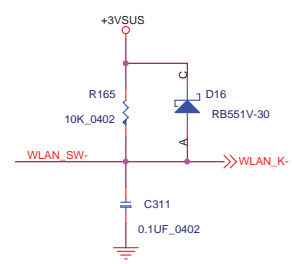
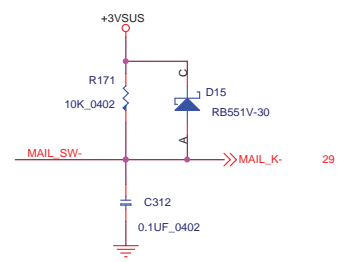
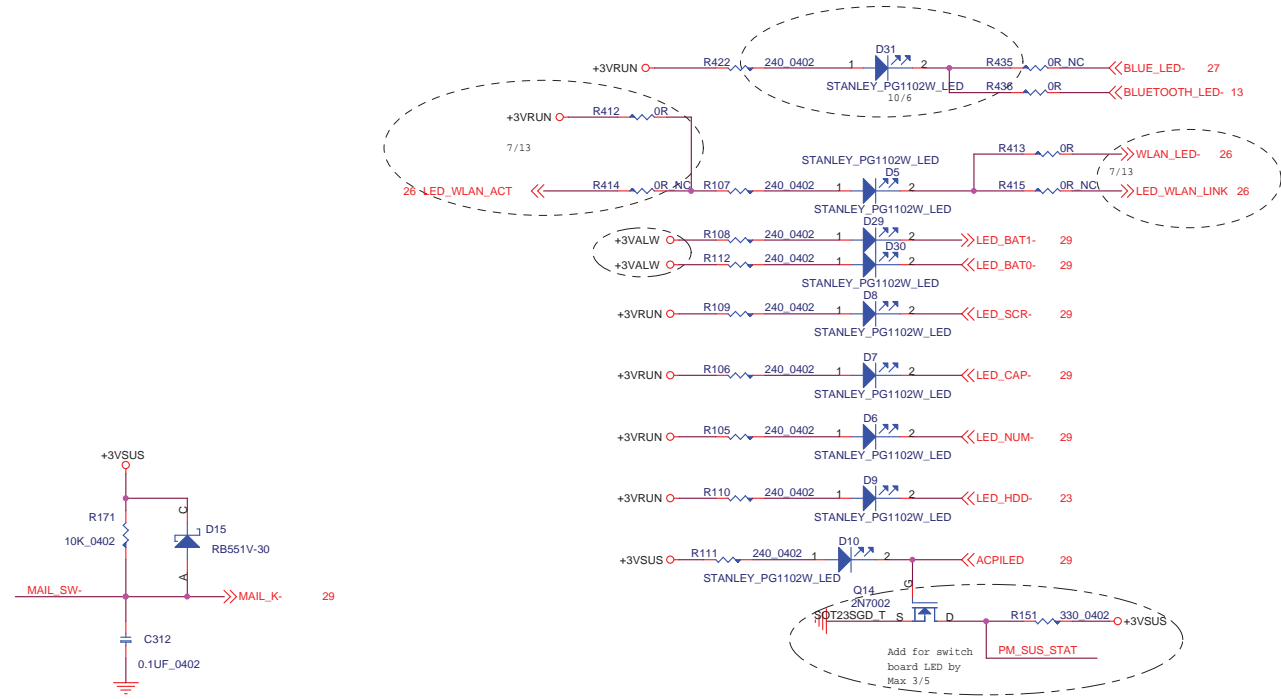
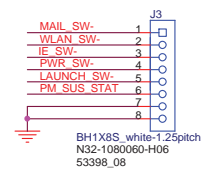
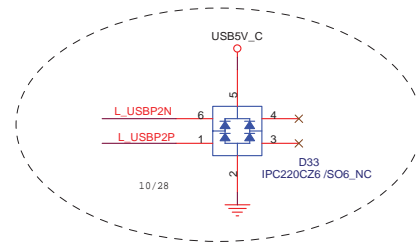
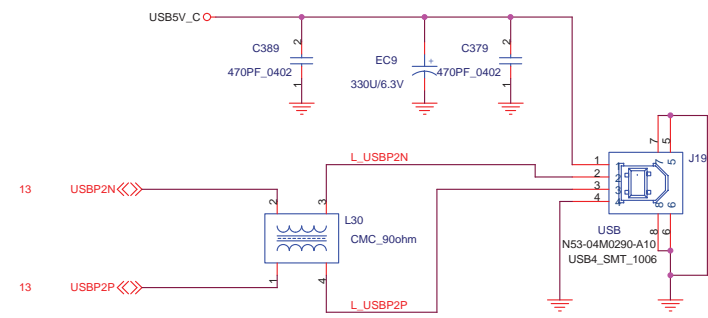
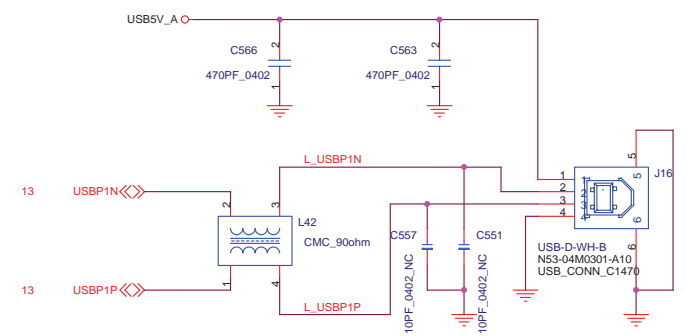
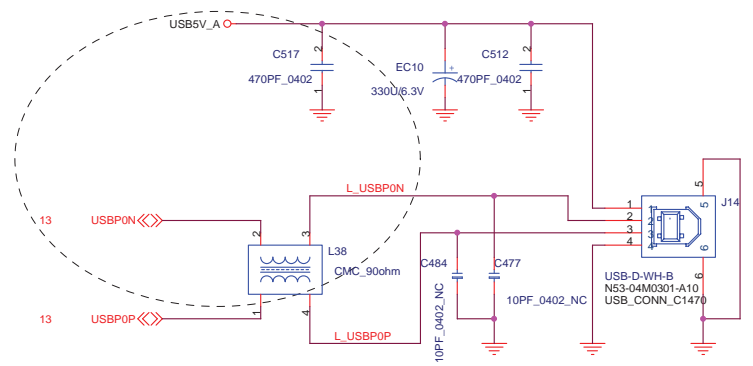
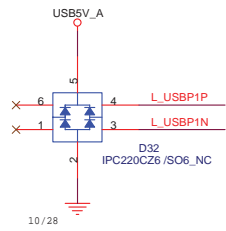
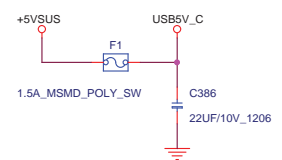
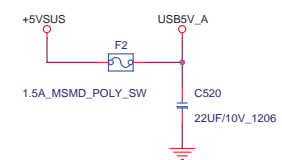
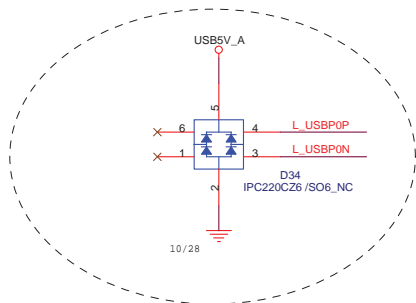


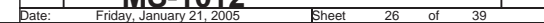


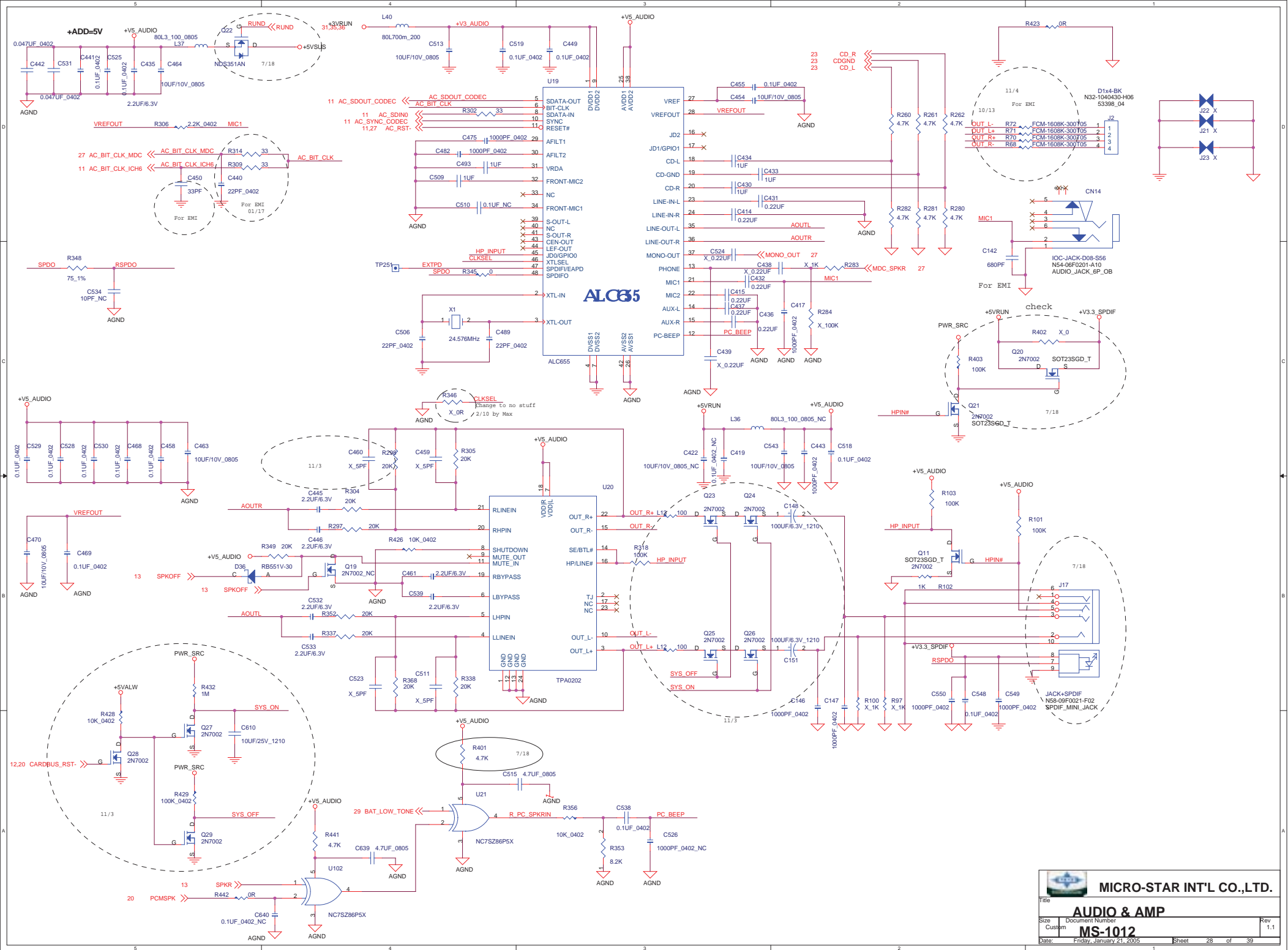
PIN32:PDIAG
PIN37:PASP
PIN47:CABLE SELECT

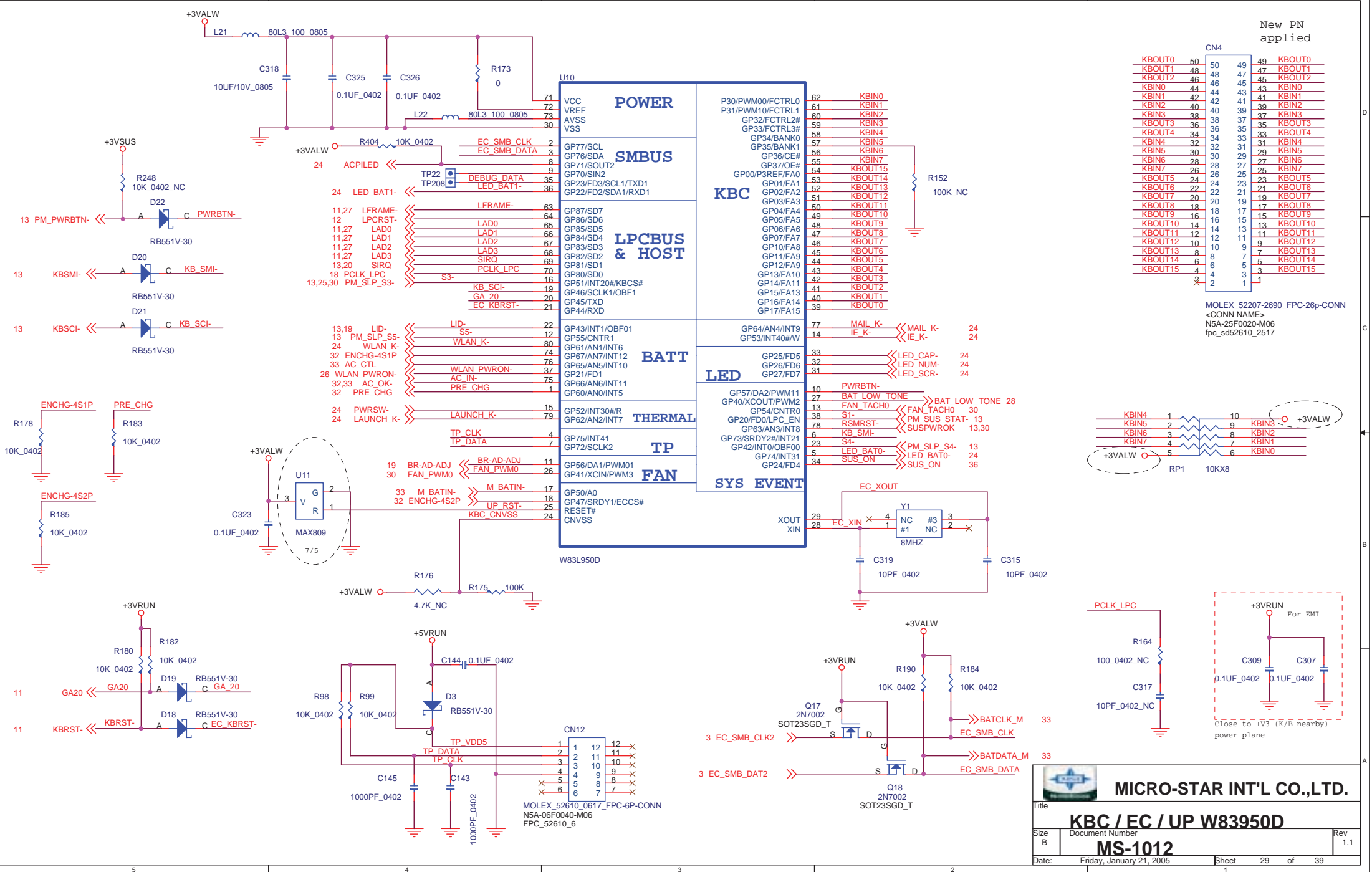



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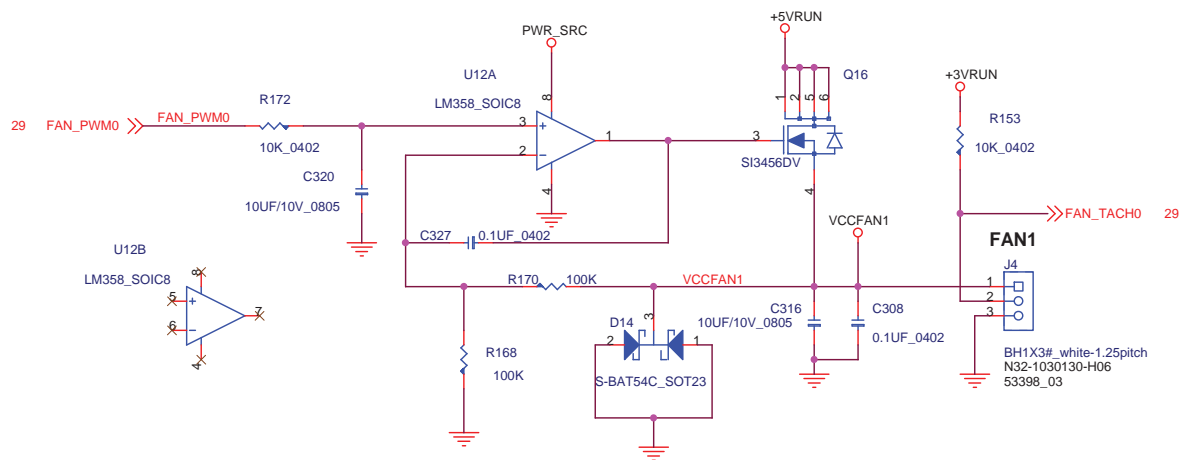
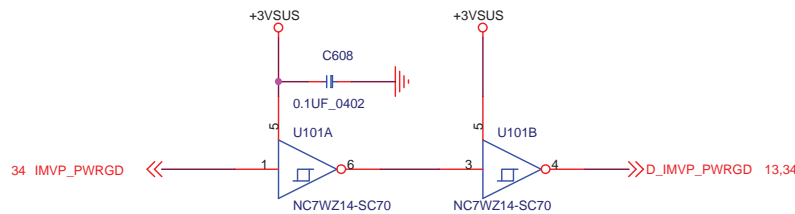
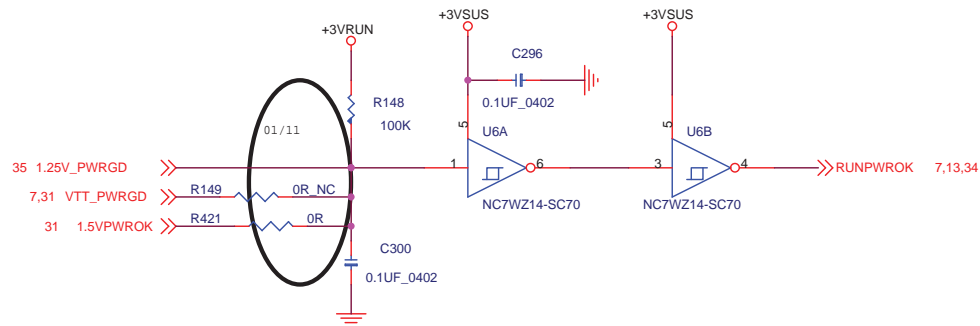
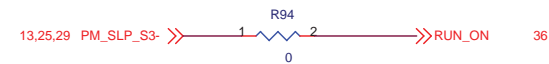
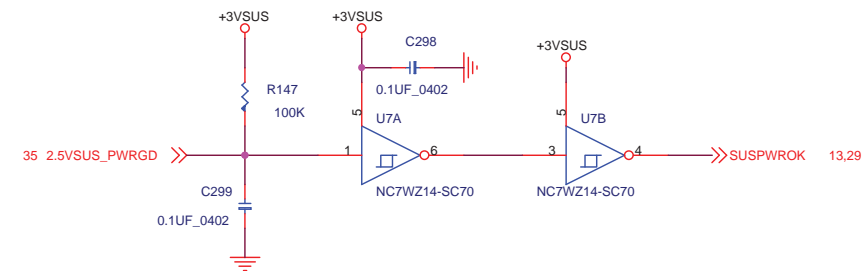
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MS-1012

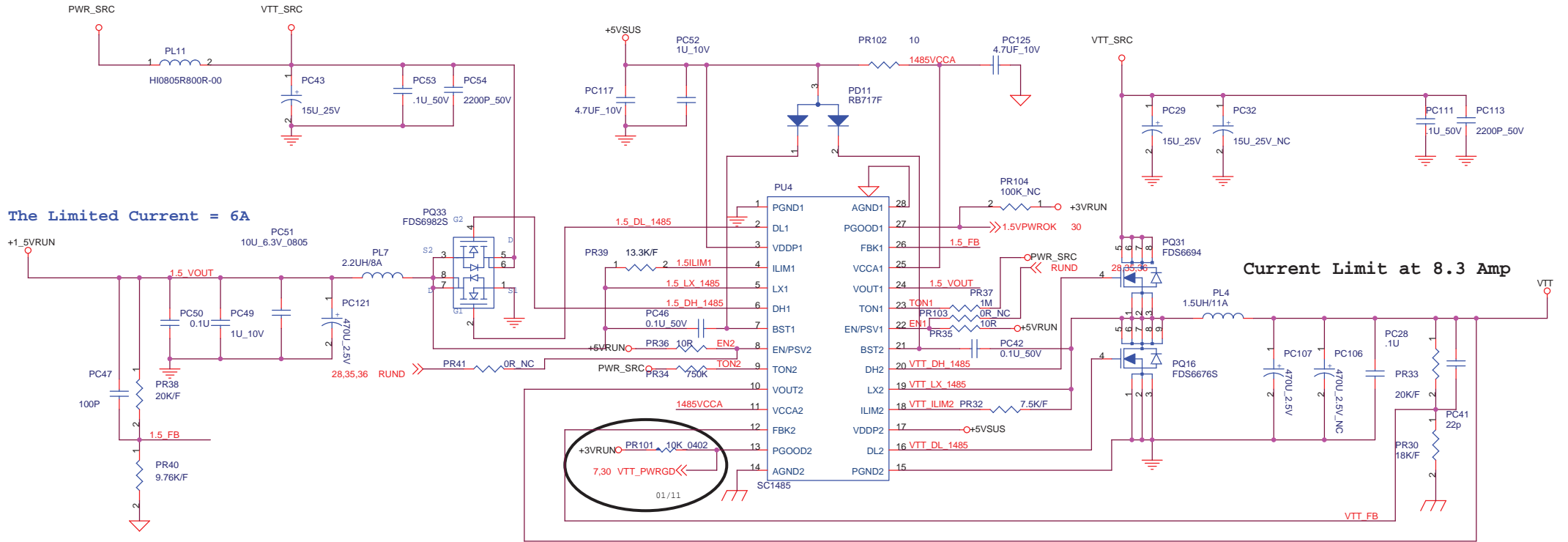
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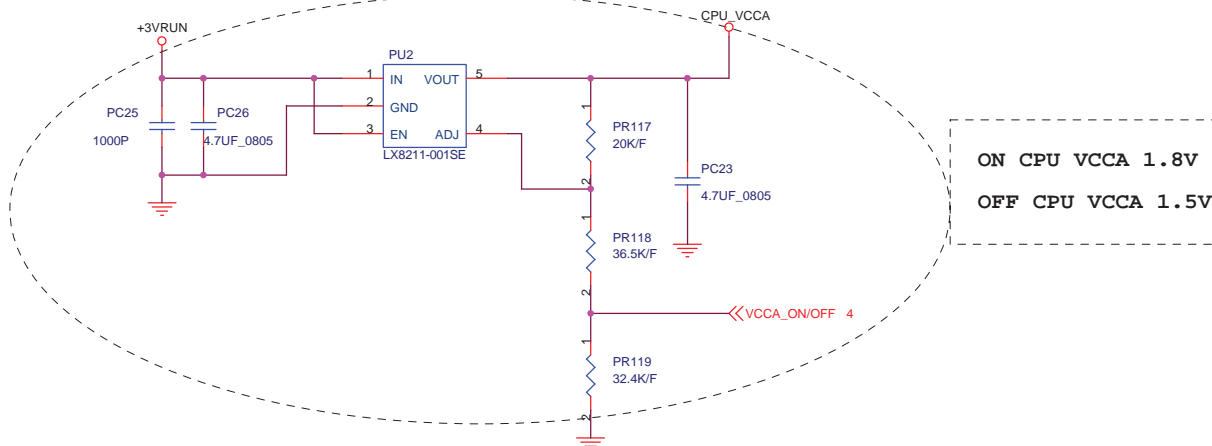
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The Limited Current = 6A



Current Limit at 8.3 Amp

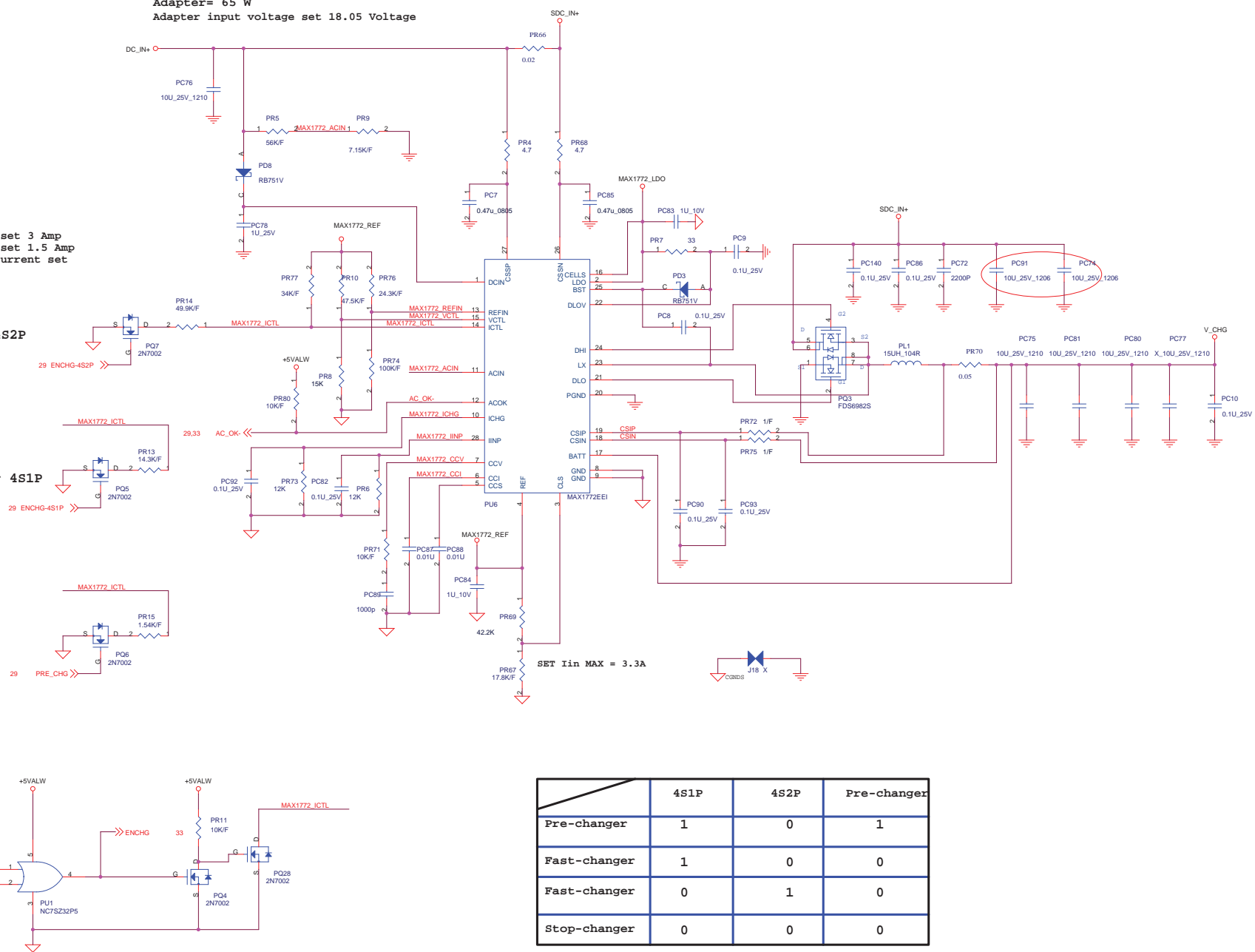


ON CPU VCCA 1.8V
OFF CPU VCCA 1.5V

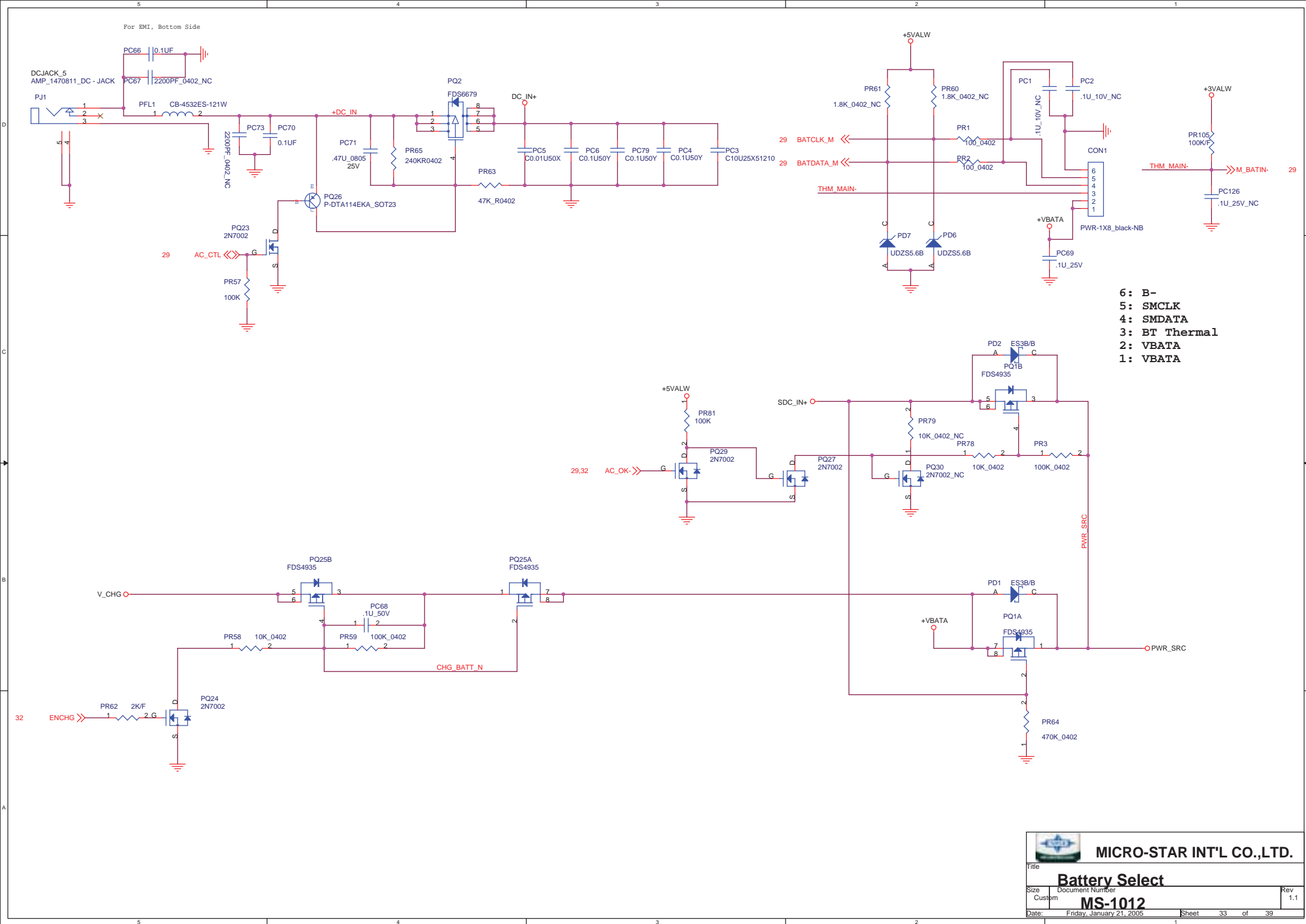
4S2P: Charger current set 3 Amp
 4S1P: Charger current set 1.5 Amp
 Pre-charger: Charger current set 200mA

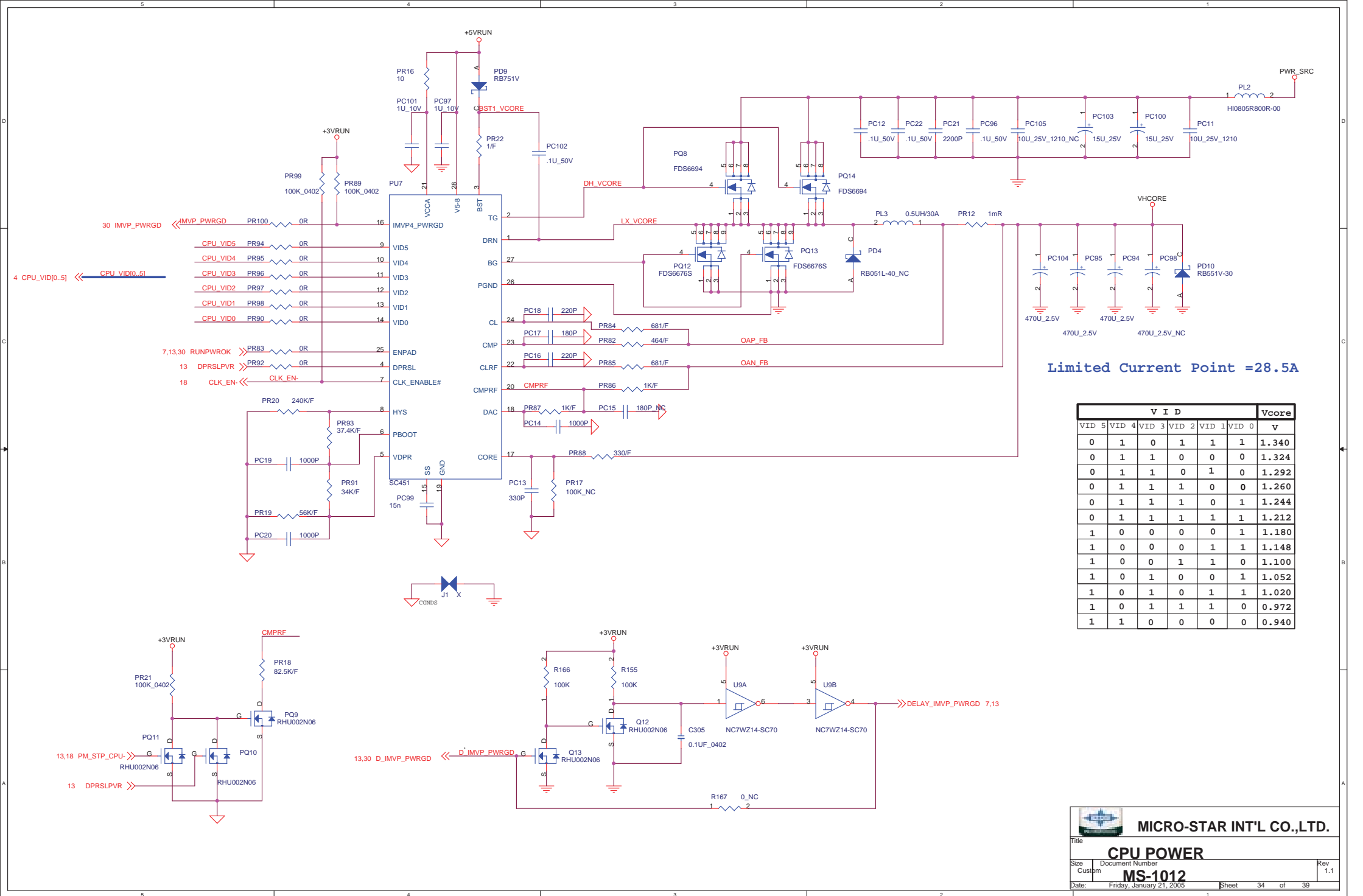
Charge to 3A for 4S2P

Charge to 1.5A for 4S1P

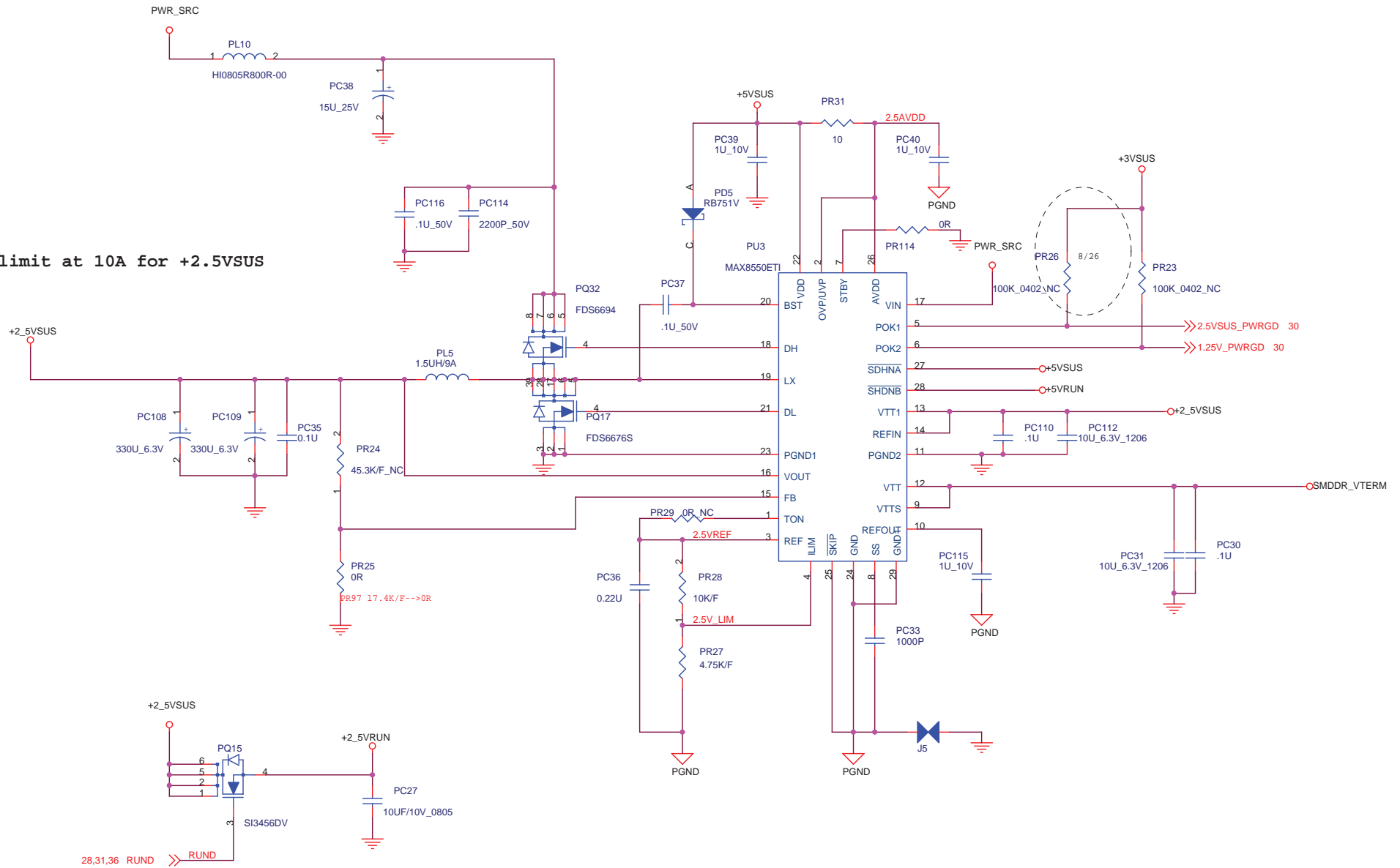



	4S1P	4S2P	Pre-charger
Pre-charger	1	0	1
Fast-charger	1	0	0
Fast-charger	0	1	0
Stop-charger	0	0	0





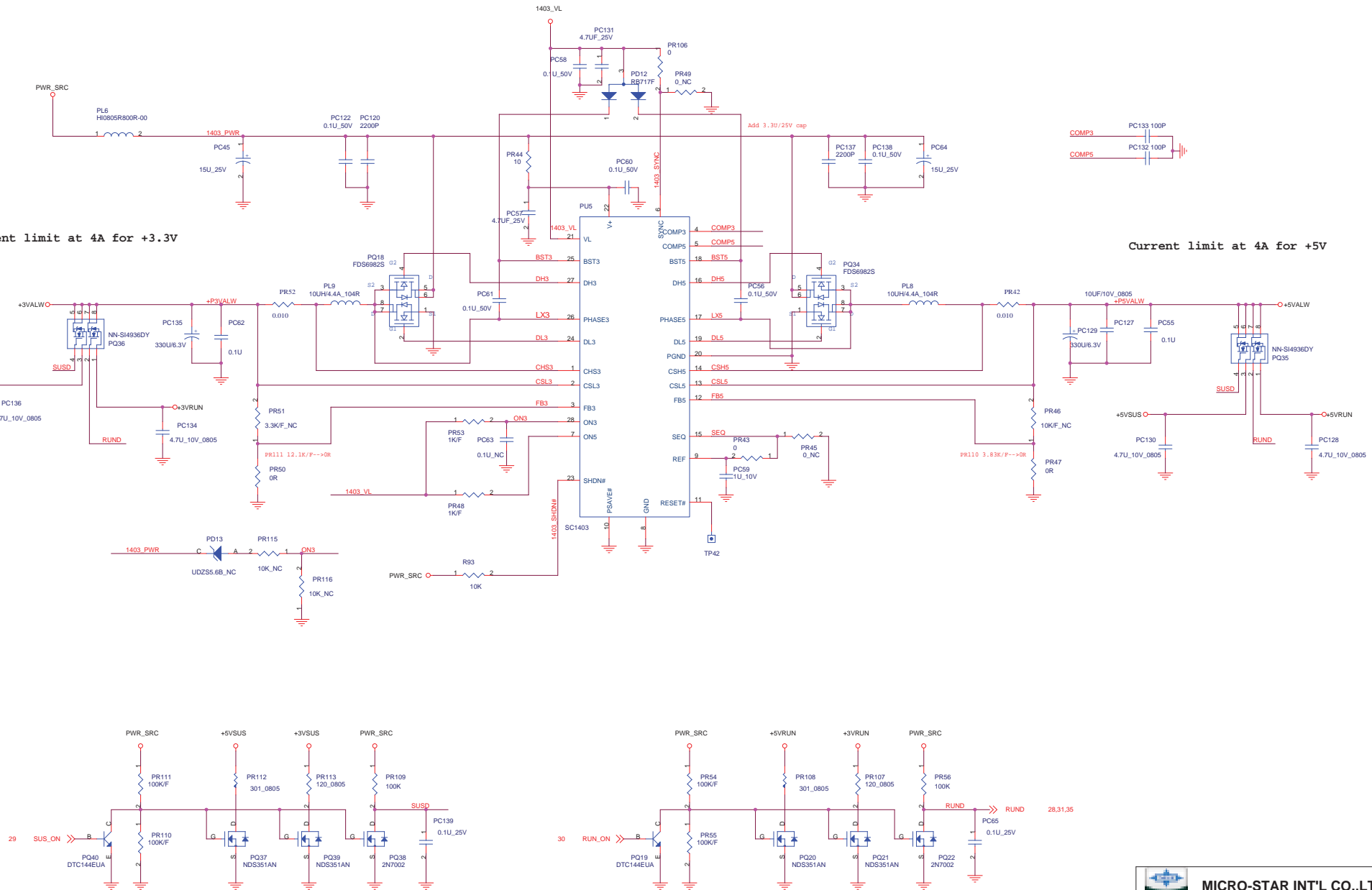
Current limit at 10A for +2.5VSUS

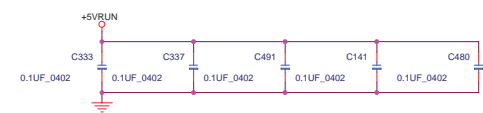
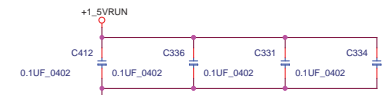
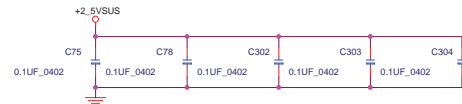
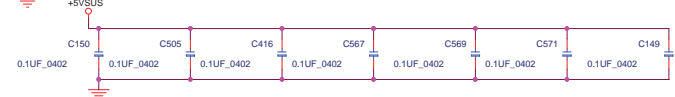
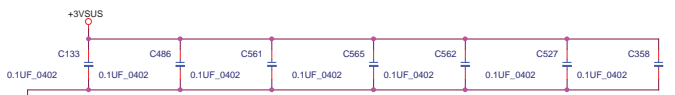
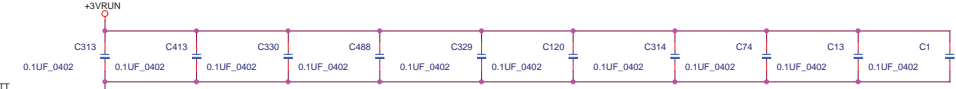
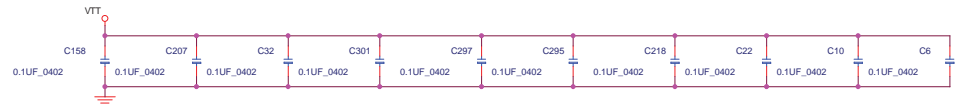
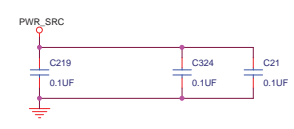
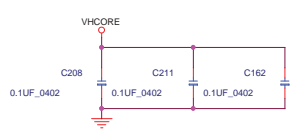
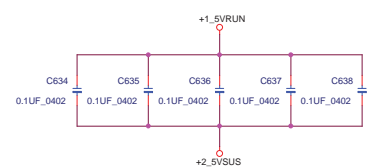
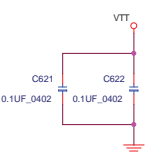
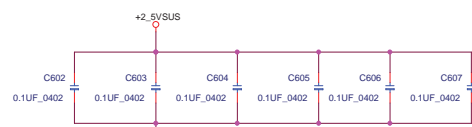
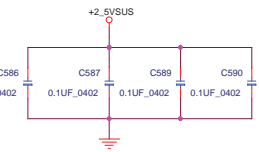
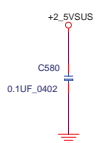
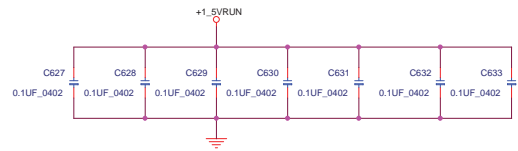
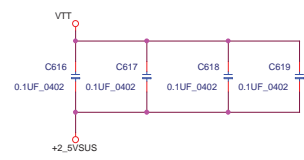
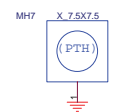
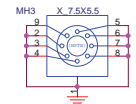
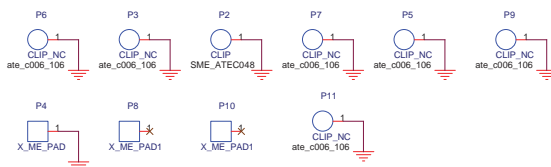
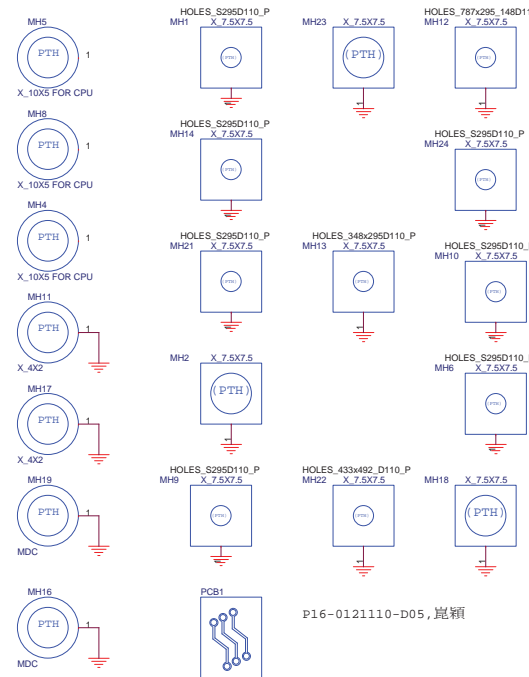


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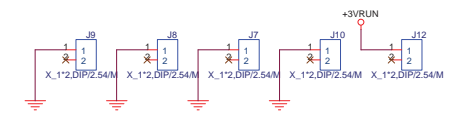
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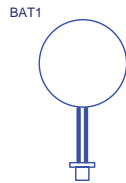
Current limit at 4A for +5V





For EMI





RTC_BAT
D06-0100300-K26



ML3
DDRMYLAR
E26-1003120-SA6



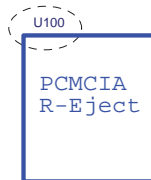
ML6
DDRMYLAR
E26-1003120-SA6



SC1
VGASC
E42-A040535-F02



SC2
VGASC
E42-A040535-F02



PCMCIA-EJECT
N5D-68M0170-T01



SHD1
PCMCIA SHIELDING
E21-1006060-Y28



ML1
SDMYLAR
E26-1006100-P38



ML4
KBMYLAR
E26-1006190-P38



ML5
KBMYLAR
E26-1006190-P38



ML2
KBMYLAR
E26-1006090-P38



SHD2
VGA SHIELDING
E21-1006020-Y28



SC3
M2X12



SC4
M2X12



SC5
M2X12



SC6
M2X12



SC7
M2X4



SC8
M2X4



MDC1
MDCASSB
S52-2801040-A95



MDCWIRE
K10-3002044-H39



ML7
HD CUSHION SPONG
E25-1012050-SE2



ML8
HD CUSHION SPONG
E25-1012050-SE2



ML9
HDD MYLAR
E26-1013010-SE2



ML10
THERMAL PAD
E26-1012040-C60



ML11
THERMAL PAD
E26-1012040-C60

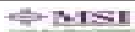


ML12
CONDUCTIVE GASKET FOR RJ11
E25-1012040-CA7

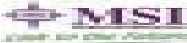


ML13
CONDUCTIVE GASKET FOR 1394
E25-1012020-CA7

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1. Modify Page7 NB_PWRGD Link to VTT_PWRGD add R443 & R444
2. Modify Page7 Delete R58 & R55 & R59
3. Modify Page13 Add R453 & R446 0 ohm NC
4. For EMI Modify Page 17
C270,C231,C284,C242,C289,C238,C273,C226,C105,C281,C290,C236
C293,C106,C278,C267,C268 Change to 0.01UF_0402 CAP
5. For MSI_6855 Wireless & Bluebooth Mini_PCI
Modify Page 26 Add R445 10K ohm & Q31 2N7002 & R451 & R452 0 ohm
6. For EMI Solution (1) Modify Page 28 R314 0 ohm change to 33 ohm
(2) Modify Page 28 add C440 22PF CAP
(3) Modify Page 28 add C450 33PF CAP
(3) Modify Page 28 add short pin J23,J2,J22
7. Modify Page 28 Delete Q19 2N7002 & add D36
8. Modify Page 30 Delete R149 0 ohm
9. For EMI Solution Modify Page 32 Add PL12 & PC140
10. For EMI Solution Modify Page 31 PR101 change to 10K_0402
11. For EMI Solution Modify Page 37 Delete P5,P6,P9
12. For EMI Solution Modify Page 33 PC67 & PC70 0.1UF_0402 CAP
13. Modify Page 28 R429 Change to 100K_0402

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